Towards subvolt and half-mm scale silicon MOS-capacitor MZI modulators

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***Abstract*—We report the demonstration of sub-mm scale silicon lateral MOS-capacitor MZI modulators operating at > 100 Gb/s PAM-4. The 3D packaged transmitter demonstrates an RF swing of 1.2Vpp and a TDECQ of 1.7 dB for MZI with a total active length of 600 µm.**

Keywords—silicon photonics, electro-optic modulators, optical interconnects, integrated optoelectronics

I-Introduction

Silicon photonics is well placed to support Tb/s-scale inter-rack and intra-rack interconnec[1]–[4] and Pb/s scale in the near future [5]. Integrated all silicon high speed optical modulators have been demonstrated as enssential components. The widely studied silicon PN junction modulator which uses the carrier depletion effect has been optimized and developed with operation up to 112 Gbaud PAM-4 for MZI modulators integrated with CMOS drivers at a power consumption of sub pJ/bit [6]. Silicon ring modulators with ultra compact size < 10 µm have also also been demonstrated at 120 Gbaud PAM-4 [7]. MZI structures are preferred in terms of wavelength independence and temperature insensitivity, while ring modulators are ultra-compact and suitable for high density integration by overcoming the resonance control over changes of temperature and laser wavelength. Alternatively, ultra-compact MZI modulators can be another option and provides the trade off of bandwidth density and wavelength insensitivities.

Here we demonstrate that 3D packaged all silicon carrier accumulation MZI modulators can pave such a way to achieve compactness (~600µm), low driving voltage (1.2Vpp) and high speed (100 Gb/s PAM-4). The carrier accumulation modulators are formed within laterally stacked polysilicon/SiO_2/Si waveguides with about 6nm oxide, and fabricated in 8-inch SOI wafers with a 220 nm silicon overlayer. The devices can reach a phase efficiency up to 0.65 V.cm in carrier accumulation mode. Experimentally, 56 Gbaud PAM-4 operation can be achived when directly driven by lumped electrodes for MZIs with two 500 µm long phase shifter segments. A small MOSCAP MZI transmitter has also been fabricated, which has two MOSCAP segments within each arm (with lengths of 200µm and 400µm). The modulator is co-designed and flip-chip bonded with a 28nm CMOS driver. The 3D packaged MOSCAP transmitter allows 100 Gb/s PAM-4 operation with a TDECQ value of 1.74 dB and a modulation extinction ratio (ER) 4 dB, which is achieved at the cost of optical loss close to 7dB and RF swing up to 1.2 Vpp for both segments.

II-Lateral MOSCAP modulators

To acheive more efficient and controllable eletro-optical phase shifters, we fabricated lateral MOSCAP waveguide phase shifters, composed of silicon/SiO_2/polysilicon, by the method described in [8]. A schematic of the MOSCAP waveguide cross-section is shown in Fig.1(a). The characterized phase change efficiency grows up to 0.65 Vcm when DC bias increases above the flat band voltage. The measured optical losses for the doped active waveguides are optimized to be 3.8 dB/mm. The modulators are designed to achieve a compact size and only requiring lumped electrodes. Co-designed CMOS drivers are flip-chip bonded with the photonics modulator chips, which also serves as the interposer for the CMOS driver, providing the required pads/wires for the input RF and DC signals.

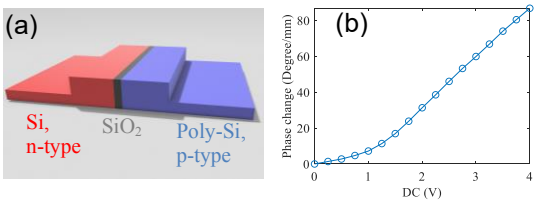

Fig.1 (a) Schematic of the MOSCAP waveguide cross-sections formed with silicon/SiO_2/poly-Si. (b) Measured phase change efficiencies VS DC bias.

The MOSCAP MZI modulators are firstly tested by sending two channel RF signals to the two segments by using 50 ohm terminated GSGSG probes as shown in Fig.2(a). For segment lengths of 500 µm, 56 Gbaud PAM-4 modulation can be achieved with an ER > 3 dB and RF voltages about 1Vpp and 2Vpp for the two segments, respectively. The bandwidth of lumped MSOCAP modulators is mainly limited by the 50 ohm source impedance and the RF traveling wave signal integrity loss when terminated at the electrodes. Hence, the quality of the measured PAM-4 optical eye

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diagram in Fig.2(b) is limited with a large noise, which means a TDECQ value of 6 dB with eye averaging and sub 1 dB when excluding noise.

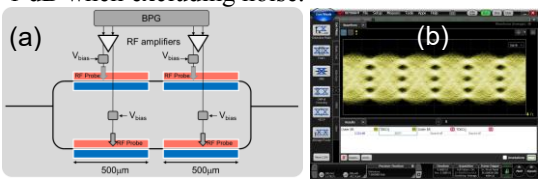

Fig.2 Schematic test setup for the segmented silicon MOSCAP MZI modulators using external Bit-Pattern-Generator, RF amplifiers, bias-Tees and RF probes (a). The measured optical eye diagram at 56 Gbaud PAM-4.

To circuvement the RF signal integrity loss and bandwidth limitations, a 28nm CMOS driver has been co-designed with source impedance less than 50 Ω and flip-chip bonded with the MOSCAP MZI modulator. The co-designed CMOS driver also provides controllable pre-distortion and inductive peaking techniques to optimize the bandwidth and power consumption [9]. The CMOS chip has two drivers channel, which are optimized for the two MOSCAP segments, respectively. The packaged transmitter allows better PAM-4 operation as shown in Fig.3(b) in comparison with the testing method used in Fig.2(a). The measured PAM-4 performance at 100 Gb/s is optimized with a TDECQ of 1.74 dB (5 taps FFE and IEEE802.bs) and ER of 4 dB as shown in Fig.3(b). The CMOS driver supplies up to 1.2 Vpp RF swing and has a power consumption of approximately 2.4 pJ/bit [9]. For 100 Gb/s operation, the inductive peaking was turned-off and pre-disortion was used to optimize the eye diagram. In comparison with travelling wave depletion modulation, the tranmistter doesn't show better optical insertion loss, which includes 3dB quandrature loss and 3-4 dB extra loss (~2.3 dB passive loss, ~1.7 dB extra bias loss below the quandrature point).

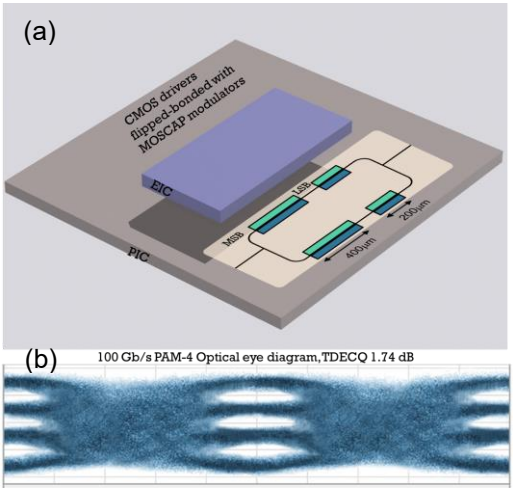

Fig.3. (a) 3D Schematic of the CMOS drivers flip-chip-bonded with MOSCAP modulators for segmented PAM-4 operation. (b) Optical PAM-4 eye diagram obtained with TDECQ filter (5-tap FFE, IEEE802.bs), showing a modulated ER of 4 dB and TDECQ of 1.7 dB.

CONCLUSIONS

Lateral MOSCAP modulators were fabricated in 220 nm SOI wafers with phase modulation efficiencies 0.65 V.cm achieved, which allows 56 Gbaud PAM-4 operation at the sub mm scale. The packaged MOSCAP transmitter, with built-in pre-distortion, inductive peaking techniques and low source impedance incorporated into a co-designed 28nm CMOS driver, has demonstrated 100 Gb/s PAM-4 operation with a TDECQ value of 1.74 dB, modulated ER of 4 dB, optical loss close to 7 dB and power consumption at approximately 2.4 pJ/bit. This work paves way to achieve subvolt and half-mm scale silicon MOS-capacitor MZI modulators with further optimization of the phase efficiency, optical loss and E/O co-design methods in the future.

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