

An AC-Coupled Wideband Neural Recording Front-End With Sub-1 mm² × fJ/conv-step Efficiency and 0.97 NEF

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Abstract—This letter presents an energy-and-area-efficient ac-coupled front-end for the multichannel recording of wideband neural signals. The proposed unit conditions local field and action potentials using an inverter-based capacitively coupled low-noise amplifier, followed by a per-channel 10-b asynchronous SAR ADC. The adaptation of unit-length capacitors minimizes the ADC area and relaxes the amplifier gain so that small coupling capacitors can be integrated. The prototype in 65-nm CMOS achieves 4× smaller area and 3× higher energy–area efficiency compared to the state of the art with 164 μm × 40 μm footprint and 0.78 mm² × fJ/conv-step energy-area figure of merit. The measured 0.65-μW power consumption and 3.1-μV_{rms} input-referred noise within 1 Hz–10 kHz bandwidth correspond to a noise efficiency factor of 0.97.

Index Terms—AC coupling, front-end, inverter-based amplifier, monotonic switching, neural recording, successive approximation register (SAR) analog-to-digital converter (ADC), unit-length capacitor (ULC).

I. INTRODUCTION

Recording and decoding high-frequency neural features through the intracortical brain–computer interfaces have allowed accurate control of complex actuators [1]. Moving from laboratory demonstrations to the widespread use of such systems requires combining signal acquisition and processing in an implantable system on chip [2], [3], under stringent energy and size constraints. Therefore, accommodating the maximum number of electrodes requires the lowest energy-area cost per recording channel.

Neural signals bear information within frequency bands called local field potentials (LFPs) up to ~300 Hz, and action potentials (APs) between 300 Hz and 10 kHz, with amplitudes typically ranging from a few μV to a few mV [4]. A generic neural recording front-end boosts, filters, and digitizes these signals using a low-noise amplifier (LNA) followed by an analog-to-digital converter (ADC) as depicted in Fig. 1(a). Traditionally, the electrodes are ac coupled to the front-end to reject large and variable dc offsets building on the tissue–electrode interface [5]. The coupling capacitor also presents a high-input impedance to the electrode, and serves as an isolation layer against static device currents and short circuits [6]. Nevertheless, the capacitor area becomes a bottleneck when a high gain and a low high-pass pole is required [7], limiting the scalability of this approach.

Several dc-coupled techniques have been proposed to eliminate bulky coupling capacitors at the expense of other circuit qualities.

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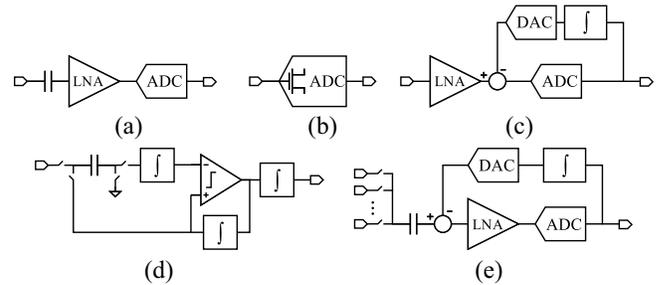


Fig. 1. (a) AC-coupled front-end architecture and dc-coupled area reduction techniques using (b) direct digitization, (c) mixed-signal offset cancellation, (d) switched-capacitor delta modulation, and (e) electrode multiplexing.

Direct digitization [Fig. 1(b)] by removing the LNA results in excessive input-referred noise (IRN) [8]. Canceling the offset through a mixed-signal feedback loop [Fig. 1(c)] [7] has a digital power and area overhead that scales up with the desired input range. Delta modulating the input with switched capacitors [Fig. 1(d)] can achieve rail-to-rail cancellation at the cost of reduced input impedance and increased noise at high sampling rates [9], which is also the case when the electrodes are multiplexed into a shared front-end [Fig. 1(e)] [10]. Moreover, the injection of switching currents into the neural tissue raises safety concerns which has not yet been addressed. Due to these fundamental limitations of dc coupling, ac-coupled front-ends are still favorable for wideband recording thanks to low noise, passive offset rejection, and high-input impedance. However, the area efficiency of this approach has to be improved to allocate more resources to other implant features.

In this letter, we present an ac-coupled neural recording front-end architecture which permits high integration density without compromising power efficiency or sampling frequency. Our adaptation of unit-length capacitor (ULC)-based successive approximation register (SAR) ADC [11] minimizes the ADC area and relaxes the LNA gain requirement, which in turn makes room for small coupling capacitors. The inverter-based LNA achieves high noise efficiency thanks to current reuse. The constant common-mode monotonic ADC switching scheme further improves the energy efficiency. Our prototype in 65-nm CMOS process achieves the smallest ac-coupled footprint reported in the literature with 6560 μm², which is also smaller than or comparable to the recent dc-coupled implementations. The overall energy-area figure of merit (E-A FoM) measuring 0.78 mm² × fJ/conv-step, as well as the noise efficiency factor (NEF) measuring 0.97 within 1 Hz–10 kHz bandwidth, are below the state of the art.

II. DESIGN DETAILS

The proposed front-end follows the conventional approach depicted in Fig. 1(a). A capacitively coupled LNA (CC-LNA) boosts and filters neural signals within LFP and AP bands, followed by a 10-b 20 kS/s ULC-based SAR ADC. The following sections provide detailed descriptions of each part.

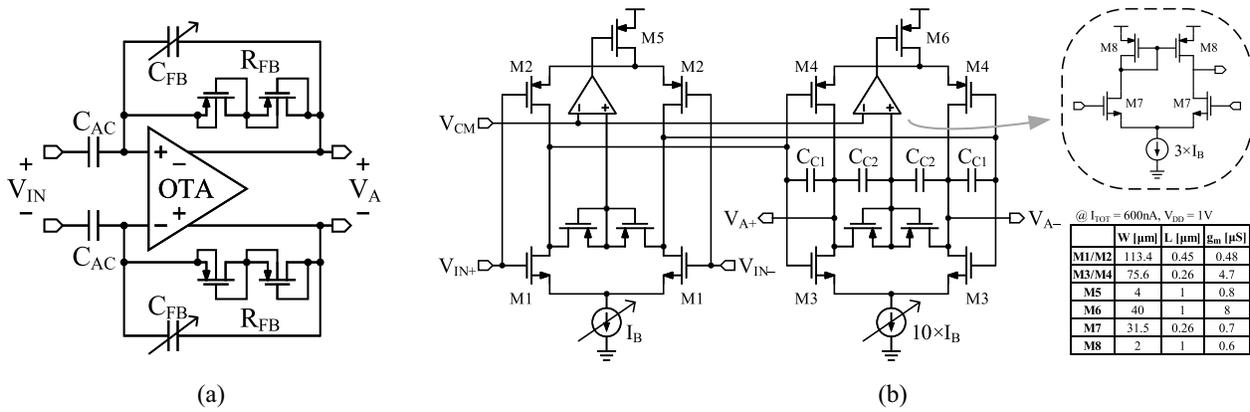


Fig. 2. (a) Fully differential CC-LNA. (b) Transistor-level schematic of the two-stage inverter-based OTA.

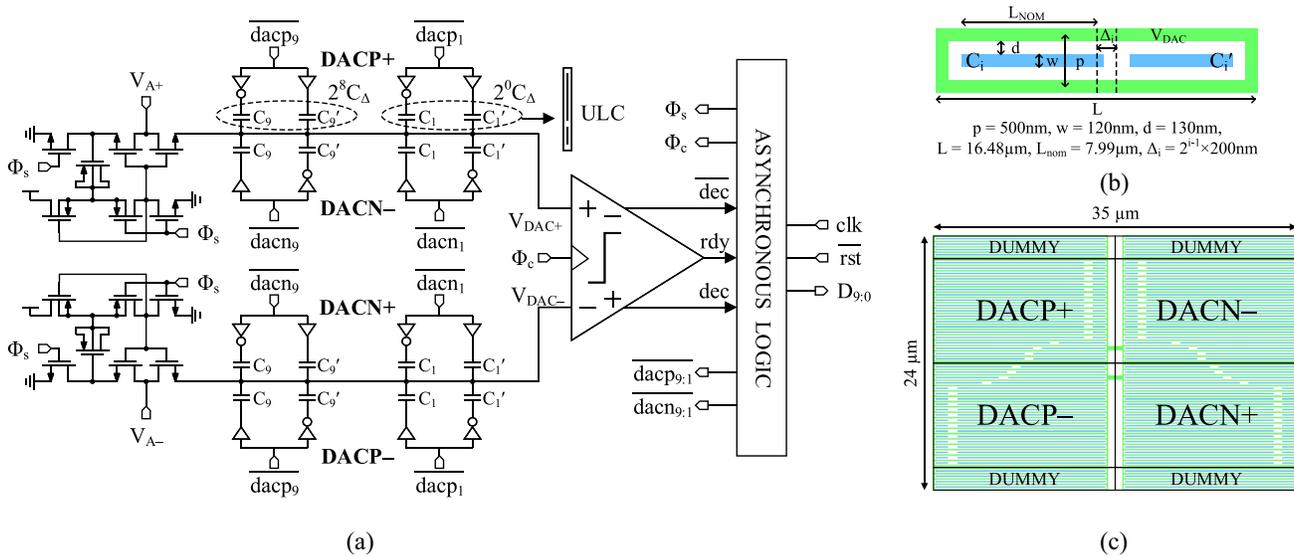


Fig. 3. (a) Detailed schematic of the ULC-SAR ADC showing the bootstrapped switch and constant common-mode ULCDAC circuits explicitly. (b) ULC dimensions following the naming convention in [11]. (c) Physical implementation of the differential constant common-mode ULCDAC.

A. Capacitively Coupled Low-Noise Amplifier

Fig. 2(a) shows the CC-LNA schematic. The nominal gain of the amplifier is set by the capacitor ratio C_{AC}/C_{FB} as 40 dB, based on the ADC input range and the expected recording site noise as will be discussed in Section II-B. We choose C_{AC} as 2 pF, and C_{FB} can be configured from 15 to 65 fF corresponding to 30–40-dB programmable gain. Diode-connected pMOS feedback resistors (simulated nominal $R_{FB} = 50$ TΩ) ensure that the high-pass cut-off at $1/(2\pi R_{FB} C_{FB})$ stays below 1 Hz for all configurations of C_{FB} across corners. The low-pass cut-off can be adjusted by changing the bias current (I_B) of the operational transconductance amplifier (OTA).

The fully differential OTA employs the two-stage inverter-based topology shown in Fig. 2(b). This topology has high noise efficiency thanks to the current being reused by the complementary differential pairs. All pairs are constructed with thick-oxide transistors and operate in a weak inversion regime, hence the open-loop gain depends mostly on transistor lengths. The first stage provides 38-dB gain, the second stage adds 25 dB and drives the ADC input. The output common mode is sensed via diode-connected transistors and set nominally to $V_{DD}/2$ by a simple common-mode feedback (CMFB) amplifier. Compensation capacitors ($C_{C1} = 240$ fF, $C_{C2} = 35$ fF) and the ratio of tail currents ensure stability in all corners.

B. ULC-Based Asynchronous SAR ADC

The amplified signals are digitized by the 10-b 20-kS/s asynchronous SAR ADC shown in Fig. 3(a). The key area advantage of the ADC is the ULC-based digital-to-analog converter (ULCDAC), first proposed in [11]. A ULC relies on the difference of two metal capacitors ($C - C' = 2C_{\Delta}$) with unit length difference Δ , such that a binary weight can be realized by adjusting C_{Δ} rather than multiplying the capacitor structure. As a result, the total array requires N ULCs instead of 2^N unit capacitors. Moreover, the ULCDAC can be constructed using a few metal layers and placed above the other circuits. Fig. 3(b) illustrates the ULC used in this implementation with its construction parameters following the conventions in [11]. The plates are constructed in M6 and M7 layers in parallel, which results in 0.1 fF C_{Δ} .

Our adaptation of ULCDAC shown in Fig. 3(c) leverages the constant common-mode monotonic switching scheme [12] to reduce the switching activity while maintaining a constant common-mode voltage for the comparator input. This requires a second ULCDAC switching in the opposite direction, but brings no area overhead as the single ULCDAC size is halved thanks to monotonic switching. As a result, the overall differential DAC consists of four single-ended ULCDACs, each of which is partitioned into 4-b binary LSB and 4-b unary MSB arrays to keep mismatch under control as explained

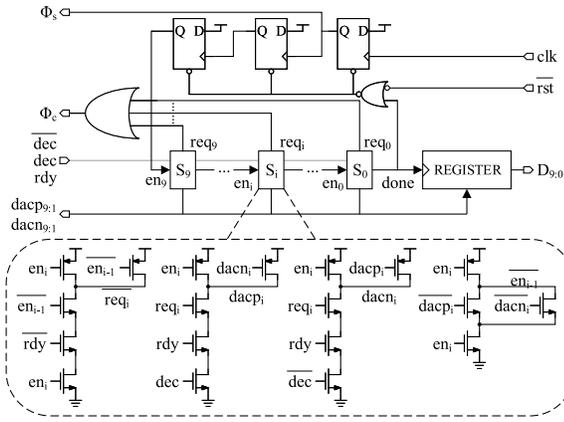


Fig. 4. Asynchronous logic for monotonic switching algorithm.

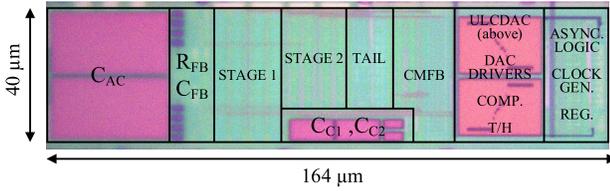


Fig. 5. Annotated micrograph of the $164 \mu\text{m} \times 40 \mu\text{m}$ prototype.

in [11]. The remaining two bits are implicit as the first comparison is performed on the sampled input, and the last two bits are implemented single ended. Although the benefit of energy-efficient switching on the small capacitance of ULCDAC is negligible [11], we observe 10% reduction in total simulated ADC power thanks to less activity in the asynchronous logic block.

Another feature of ULCDAC useful for our application is that, due to the total capacitance ($\Sigma(C + C')$) being higher than the total effective differential capacitance ($\Sigma(C - C')$) [11], the input range of the ADC decreases from 2 to 0.65 V peak-to-peak differential without needing a separate supply or dedicated reference generators. The resulting 0.6-mV quantization step allows us to choose 40-dB LNA gain to capture signal content above the $5\text{-}\mu\text{V}_{\text{rms}}$ expected measurement noise floor [6].

The switches, comparator, and DAC drivers are placed below the ULCDAC with shielding in M4 and M5 layers. To reduce sampling nonlinearity, bootstrapped track and hold switches were used where a pMOS precharge capacitor is used to save area. The comparator employs a dynamic double-tail architecture [11]. Fig. 4 shows the asynchronous logic for the proposed ADC. Upon a rising external clock edge, the input is sampled (Φ_s), and the chain of ten stages is initiated. Each stage clocks the comparator (Φ_c), then monotonically switches the ULCDAC depending on the decision. The conversion takes about 100 ns, and the ADC remains idle until the next clock edge which displays a low average power consumption when the sampling rate is in the order of kS/s. The circuit is a hybrid implementation of dynamic and static CMOS logic to achieve low power and robustness.

III. MEASUREMENT RESULTS

The annotated micrograph of the fabricated prototype in the 65-nm 6X1Z1U LP CMOS process is given in Fig. 5. The total channel area is $164 \mu\text{m} \times 40 \mu\text{m}$ ($6560 \mu\text{m}^2$) and the ULC-based SAR ADC takes $45 \mu\text{m} \times 35 \mu\text{m}$ ($1575 \mu\text{m}^2$).

Fig. 6(a) and (b) verifies the desired amplifier response for different gain and bandwidth settings, respectively. The gain can be modified

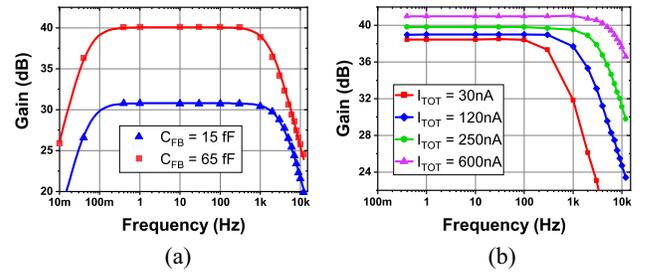


Fig. 6. Measured LNA Bode plots for different (a) gain and (b) bandwidth configurations.

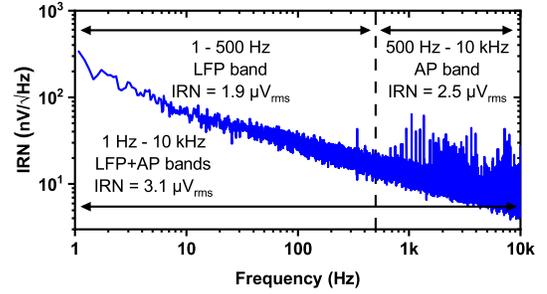


Fig. 7. Measured IRN spectrum of the front-end.

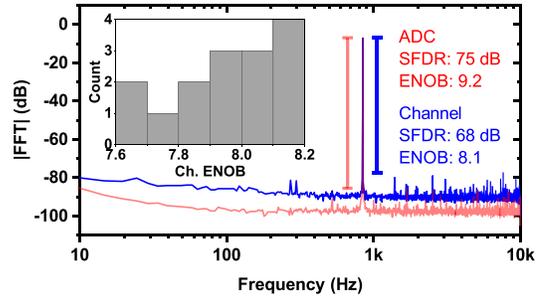


Fig. 8. Measured output frequency spectrums for the (a) ADC alone and (b) overall channel.

between 30.8 and 40.1 dB by trimming the feedback capacitor C_{FB} . The high-pass cut-off frequency is around 0.05 Hz. The bandwidth can be adjusted between 500 Hz and 10 kHz by changing the bias current, which corresponds to 30 and 600 nA total supply current from 1-V supply, respectively. The total harmonic distortion (THD) is 1.1% when 8-mV peak-to-peak differential input applied with maximum gain, and the common-mode rejection ratio (CMRR) is 56 dB. As shown in Fig. 7, the IRN over the maximum bandwidth is $3.1\text{-}\mu\text{V}_{\text{rms}}$.

The ADC consumes 47 nW when operating at 20 kS/s, and the consumption scales linearly with the sampling rate. The input range of the ULC array was measured to be 0.69-V peak-to-peak differential. The standalone ADC is able to achieve 75-dB spurious-free dynamic range (SFDR) and 9.2 effective number of bits (ENOB) over the entire bandwidth up to 2.5 MS/s.

The output spectrum of the complete channel in comparison with the standalone ADC response is given in Fig. 8. The channel performance reduces to 8.1 ENOB and 68-dB SFDR when the LNA is connected. This is due to the LNA increasing the overall noise floor, and the increased nonlinearity due to the settling of the LNA output being slightly slower than expected. The histogram in the inset of Fig. 8 depicts the interdie variation of ENOB across 15 measured samples which reflects the ULC mismatch. These could be improved with a small resource penalty by increasing the LNA drive

TABLE I
SYSTEM SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RECORDING ICs

	JSSC'12 [7]	JSSC'15 [13]	JSSC'17 [9]	JSSC'18 [4]	SSCL'18[14]	JSSC'18 [8]	TBCAS'19 [15]	TBCAS'20 [10]	This work
Technology	65nm	65nm	130nm	180nm	65nm	180nm	180nm	65nm	65nm
V _{DD} [V]	0.5	1	1.2	0.5 / 1	0.6	1.8	0.5	2.5 / 0.5	1
Coupling	DC	AC	DC	AC	DC	DC	AC	DC	AC
Multiplexing	No	Yes	No	No	No	No	No	Yes	No
Bandwidth [Hz]	10-10k	10-8k	0.01-500	0.4-10.9k	0.1-500	0-10k	1-6.8k	1-1k	0.05-10k
Sampling rate [kS/s]	20	20	1 ¹	25	1	20	31.25	2	20
IRN [μ Vrms]	4.9	7.5	1.13	3.32	2.2	12.07 ¹	5.4	1.66	3.1
NEF/PEF	5.99/17.96	4.45/12.9	2.86/9.82 ¹	3.02/4.56	8.7/45.4	29.1 ¹ /1529 ¹	2.99/4.46	2.21/12.21 ¹	0.97/0.94
ADC topology	VCO	SAR	Δ - $\Delta\Sigma$	Δ - $\Delta\Sigma$	VCO $\Delta\Sigma$	OTA-C $\Delta\Sigma$	Δ -SAR	Δ -SAR	SAR
Area/Channel [mm ²]	0.013	0.0258	0.013 ²	0.058 ³	0.01 ²	0.0049 ²	0.16 ³	0.0023 ³	0.00656
Power/Channel [μ W]	5.04	1.84	0.63 ²	3.05 ³	3.2 ²	39.14 ²	0.88 ³	2.98 ³	0.65
Resolution [ENOB]	7.2 ⁴	8.2 ⁴	11.7 ¹ @130Hz	10.3@1kHz	8.18 ¹ @40Hz	8.2@1kHz	7.7 ⁴	8 ⁵	8.1
ADC FoM _W [fJ/c-s]	84	4.25 ¹	n/a	35.2	n/a	n/a	19.6	23.32 ¹	4.0
Channel FoM _W [fJ/c-s]	1713.9 ¹	312.86 ¹	189.36 ¹	108.83	11034 ¹	7180	135.43 ¹	5820 ¹	118.5
E-A FoM [fJ mm ² /c-s]	22.28 ¹	8.07 ¹	2.46 ¹	6.34	110.34 ¹	35.182 ²	21.67 ¹	13.39 ¹	0.78

¹ Estimated from given data. ² On-chip decimation filter. ³ Off-chip decimation filter. ⁴ ADC only. ⁵ Above 200Hz.

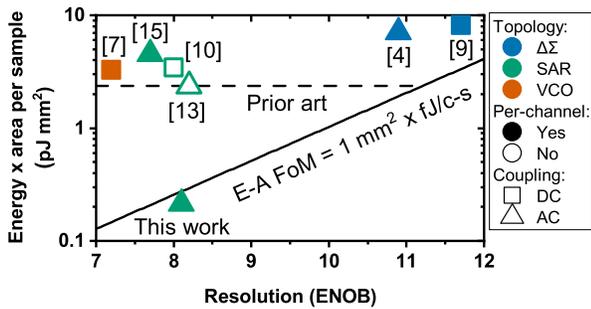


Fig. 9. Energy–area efficiency comparison with prior art.

strength and increasing ULC Δ if necessary, but the measured worst case performance still facilitates the 50-dB neural dynamic range [7].

Table I summarizes the performance of the proposed neural recording front-end and compares it with the previous works [4], [7]–[10], [13]–[15]. The silicon footprint is four times smaller than the smallest ac-coupled front-end reported, and it is comparable to the recent dc-coupled ones. The power consumption is the lowest among the wideband front-ends, which results in channel noise and power efficiency factors (NEF/PEF) [7] slightly below 1. The Walden figure of merit (FoM_W) for the ADC and the channel align with the other energy-efficient architectures. The combined energy and area efficiency improves the E-A FoM (Area × FoM_W) [4] by three times over the state of the art. In other words, the energy-area cost per sample (power × area / sampling rate) is 12 times lower than that of other similar resolution front-ends as visualized in Fig. 9.

IV. CONCLUSION

Scaling the area of ac-coupled front-ends has been challenging but essential for high-density, wideband neural signal recording with advanced on-chip processing capabilities. In this letter, we have presented such front-end based on an area-efficient ULC-based asynchronous SAR ADC and a noise-efficient inverter-based CC-LNA. The prototype fabricated in 65-nm CMOS occupies 6560 μm^2 , consumes 0.65 μW , and achieves 8.1 ENOB with 3.1- μ V_{rms} IRN within the LFP+AP band. As a result, the proposed system achieves better noise and energy–area efficiency than previously reported front-ends with 0.97 NEF and 0.78 mm² × fJ/conv-step E-A FoM. The reduction in the unit energy–area cost points toward higher channel counts and more integrated functionality within resource-constrained implants.

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