A 16-Channel Neural Recording System-on-Chip With CHT Feature Extraction Processor in 65-nm CMOS

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***Abstract*— Next-generation invasive neural interfaces require fully implantable wireless systems that can record from a large number of channels simultaneously. However, transferring the recorded data from the implant to an external receiver emerges as a significant challenge due to the high throughput. To address this challenge, this article presents a neural recording system-on-chip that achieves high resource and wireless bandwidth efficiency by employing on-chip feature extraction. Energy–area-efficient 10-bit 20-kS/s front end amplifies and digitizes the neural signals within the local field potential (LFP) and action potential (AP) bands. The raw data from each channel are decomposed into spectral features using a compressed Hadamard transform (CHT) processor. The selection of the features to be computed is tailored through a machine learning algorithm such that the overall data rate is reduced by 80% without compromising classification performance. Moreover, the CHT feature extractor allows waveform reconstruction on the receiver side for monitoring or additional post-processing. The proposed approach was validated through *in vivo* and off-line experiments. The prototype fabricated in 65-nm CMOS also includes wireless power and data receiver blocks to demonstrate the energy and area efficiency of the complete system. The overall signal chain consumes 2.6 μW and occupies 0.021 mm^2 per channel, pointing toward its feasibility for 1000-channel single-die neural recording systems.**

***Index Terms*— Compressed Hadamard transform (CHT), implantable system-on-chip (SoC), machine learning (ML), neural recording, resource efficiency, seizure detection, spreading depolarization (SD), wireless power and data transfer (WPDT).**

I. Introduction

INVASIVE brain recordings can provide insight into neural mechanisms with high spatiotemporal resolution. They have been utilized to identify biomarkers for the treatment of neurological disorders, such as epilepsy and Parkinson's disease. Moreover, these recordings are instrumental for emerging brain–machine interfaces that can restore lost motor functions in paralyzed patients [1]–[5].

Despite the promise of invasive brain recording, the translation of its applications from proof-of-concept to clinical therapies is a slow process. This is partly due to the fact that the standard clinical practice requires the implanted electrodes to be tethered to external instruments, limiting patient mobility and posing infection risks. Therefore, wireless neural recording systems have started to gain attention as a more practical alternative [6].

A straightforward wireless neural recording system transmits the raw data generated by the sensing front end to an external receiver, as illustrated in Fig. 1(a). However, as the number of channels reaches beyond 1000 [7], [8], the wireless transmission of a large amount of data emerges as a great challenge due to the limits of the available wireless standards. To illustrate, a 1000-channel system with 10-bit resolution and 20-kS/s sampling rate produces 200-Mb/s throughput, whereas the bandwidth supported by off-the-shelf implant-grade components is below 1 Mb/s [9], and the reported values in the literature can reach only up to tens of Mb/s [10].

Compression methods for neural signals have focused on reducing the data rate with acceptable loss in visual quality. Threshold coding [11], [12] is a common method that discards the low-energy spectral components to save bandwidth. However, due to the low-pass nature of neural signals, it eliminates mostly high-frequency components, which may carry significant information during a neural event. Another

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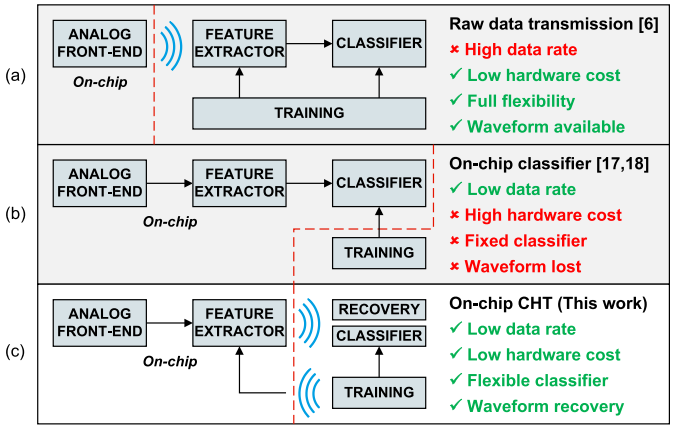


Fig. 1. Comparison of the previous and proposed neural recording approaches. (a) Raw data transmission. (b) On-chip classification. (c) On-chip CHT.

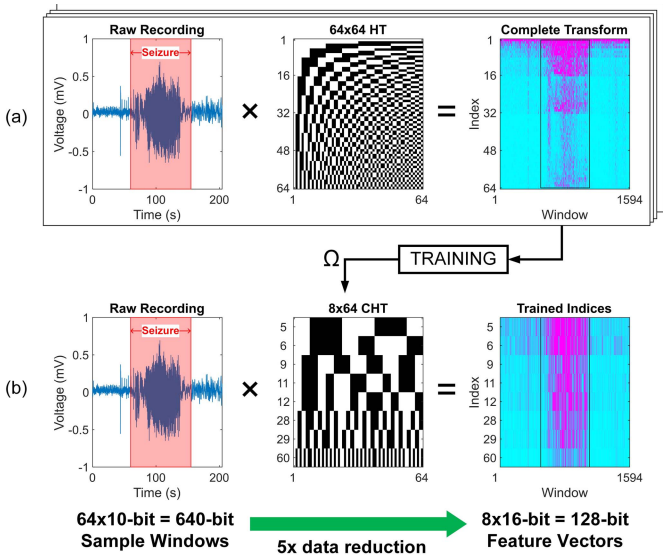


Fig. 2. (a) Seizure event within a raw recording can be identified from its HT. (b) Selecting eight of the most descriptive indices (Ω) via training on an example dataset forms the CHT. The resulting data volume is reduced by five times.

method is compressed sensing (CS) [13], [14] where fewer samples are transmitted than prescribed by Shannon's sampling theorem. Nevertheless, the recovery of the signal requires solving an underdetermined system of equations, which is prone to producing artifacts. Such losses or corruptions may adversely affect the performance of the subsequent detection algorithms even though the visual fidelity is high on average.

Given the dimensionality of multichannel neural signals and their implicit relationship with the target outcome, machine learning (ML) has gained popularity as the end user of the recordings [5], [15], [16]. Therefore, recent efforts have focused on implementing on-chip classifiers, as depicted in Fig. 1(b). Although this approach would process the raw signals locally and eliminate the need for high-rate data transmission, an on-chip ML implementation requires a large silicon area due to intensive computations and memory needs, even with a simple algorithm and a moderate number of channels. To illustrate, the single-die demonstration in [17] allocated 3.31 mm^2 to classify seizures from 32 channels, which accounted for more than half of the total chip area. In [18], a separate 3.5-mm^2 chip was dedicated to classification, in addition to the eight-channel sensing front-end chip. Limited flexibility is also a disadvantage for on-chip classification hardware since the algorithm has to be optimized and fixed at the implant level.

Extracting multichannel information from large-scale neural recording systems is an outstanding challenge due to the information loss in compression and the hardware cost of on-chip ML. To this end, we propose a neural recording system-on-chip (SoC) with an on-chip feature extractor that achieves 80% data reduction over raw data transmission while preserving the application-specific information content of the transmitted neural recordings. As depicted in Fig. 1(c), the features to be extracted by the SoC are determined by jointly training the on-chip feature extractor and the off-chip classifier on patient-specific datasets, which has not yet been explored to the best of our knowledge. Consequently, the transmitted data do not suffer from information loss and maintain over 90% sensitivity in classification at the reduced data rate. Moreover, the proposed compressed Hadamard transform (CHT) features can still be used for waveform reconstruction at the receiver side with a 23-dB signal-to-noise ratio (SNR).

The scalable data path of the SoC combines the analog front end (AFE) presented in [19] with a CHT feature extraction processor in a per-channel arrangement. The CHT processor decomposes the raw signal into its spectral components with much lower energy and area cost compared to previous feature extraction methods due to its hardware-friendly nature. The SoC also includes wireless power and data transfer (WPDT) blocks to demonstrate the overall cost of recording from sensing to transmission. The 2.9-μW power and 0.021-mm^2 area consumption per channel demonstrate the feasibility of the proposed approach for neural recording systems with over 1000 channels.

This article expands the work presented in [20] by providing a detailed description of the CHT concept, its application as a neural feature extractor and/or data compressor, and its hardware implementation. The organization of the article is given as follows: Section II introduces the CHT concept and its use in neural signal processing. Section III describes the proposed system architecture and its building blocks, namely, the AFE, the CHT processor, and the WPDT subsystem. Section IV presents the *in vivo* and off-line experimental results for waveform reconstruction, epileptic seizure detection, and spreading depolarization (SD) event identification. Finally, Section V summarizes and concludes the study.

II. Compressed Hadamard Transform

Many neural recording applications, such as speech synthesis, seizure detection, and adaptive deep brain stimulation, use spectral band energies as biomarkers [4], [15], [21]. Conventionally, these features can be extracted on-chip using finite impulse response (FIR) filter banks, fast Fourier transform (FFT), or discrete wavelet transform (DWT) processors [17], [18], [22], which are expensive computations that require

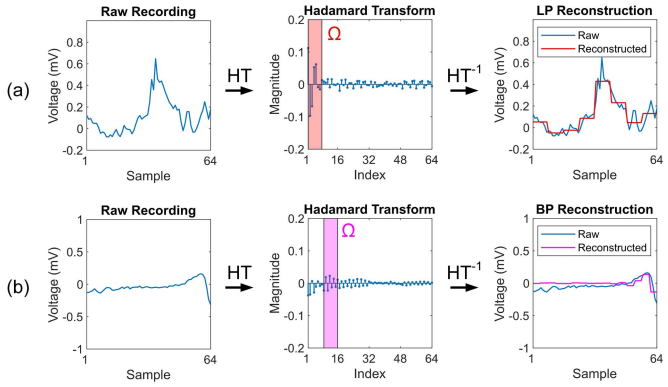


Fig. 3. Illustration of the reconstruction property of the CHT features. (a) Reconstruction from the first eight indices behaves as a low-pass filter. (b) Reconstructions from higher index groups behave as bandpass filters.

many multiply-and-accumulate operations and on-chip storage for the coefficients. Therefore, these methods are not suitable for resource-constrained large-scale neural recording.

In this work, we focus on the Hadamard transform (HT) due to its significant hardware advantages. Compared to other classes of Fourier transforms, such as FFT, the main advantage of HT is that its coefficients are either $+1$ or -1, corresponding to additions or subtractions. Moreover, these coefficients can be generated on-the-fly by a logic circuit, which alleviates the need for a coefficient memory. Therefore, HT is a hardware-friendly option for extracting spectral information from neural data.

Although HT is not an exact frequency transform FFT, it still allows correlating low or high-frequency activity to a neurological outcome. Fig. 2(a) illustrates a time series containing a seizure event and its spectrogram constructed by applying a 64×64 HT on 64-sample windows. The seizure interval in this example can be clearly identified from the spectrogram due to the increased activity, especially at higher indices. Moreover, we observe that some indices exhibit a sharper contrast in energy content compared to the others. Therefore, computing and transmitting only the descriptive indices instead of the complete transform would be sufficient for classification purposes, as illustrated in Fig. 2(b).

Identifying the most descriptive indices is not straightforward given the large datasets and the patient-to-patient variability of the signals. Therefore, the correct subset must be learned via an ML algorithm that maximizes the classification performance. The selection problem can be formally described as similar to learning-based compressive subsampling (LBCS), as presented in [23]. Consider the following mathematical model where a signal $\mathbf{x} \in \mathbb{R}^N$ is converted to its compressed representation $\mathbf{y} \in \mathbb{R}^M$ with $M < N$:

$$\mathbf{y} = \mathbf{P}_\Omega \boldsymbol{H} \mathbf{x} \tag{1}$$

where $\boldsymbol{H}$ is the HT basis and $\mathbf{P}_\Omega$ is a subsampling operator that selects the rows of $\boldsymbol{H}$ indexed by the set $\boldsymbol{\Omega}$. Suppose that we have an annotated dataset where $\mathscr{X} = \{\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_k\}$ represents k different measurements and $\mathscr{Y} = \{\mathbf{y}_1, \mathbf{y}_2, \ldots, \mathbf{y}_k\}$ represents their binary annotations. The $\boldsymbol{\Omega}$ that yields the best classification performance can be found by solving the following minimization problem:

$$\hat{\boldsymbol{\Omega}} = \underset{\boldsymbol{\Omega}, |\boldsymbol{\Omega}|=M}{\arg\min} \sum_{j=1}^{k} |\mathbf{y}_j - f(\mathbf{P}_\Omega \boldsymbol{H} \mathbf{x}_j)| \tag{2}$$

where f is the classifier model. In plain words, (2) learns $\boldsymbol{\Omega}$ that extracts the most descriptive indices of the HT. We term the customized matrix $\mathbf{P}_\Omega \boldsymbol{H}$ as the CHT matrix.

Aside from dimensionality reduction and hardware simplicity, another important benefit of the CHT feature extractor is that its output can still be used to reconstruct the waveform at the receiver side by taking the inverse transform, which is a linear computation that can be performed in real time. If the set $\boldsymbol{\Omega}$ is chosen as the lowest M indices, the reconstructed waveform will be the low-pass filtered version of the raw signal, as shown in Fig. 3(a). This selection leverages the low-pass characteristic of the neural signals and, thus, retains most of the energy content. Similarly, bandpass filters can be realized by choosing higher index groups, as shown in Fig. 3(b).

III. SoC Architecture

Fig. 4 displays the block diagram of the presented integrated circuit. The system comprises 16 configurable channels, each with an individual AFE and a CHT feature extraction processor. This modular nature of the system allows it to be scaled linearly to any number of channels. Each channel can be configured to output the features computed by the CHT processor or the raw data from the AFE. The WPDT subsystem is responsible for powering the system and sending out the aggregated channel outputs via the ultra-wideband (UWB) transmitter. Sections III-A–III-C describe each building block in detail.

A. Analog Front End

The AFE amplifies, filters, and digitizes the neural signals [local field potentials (LFPs) and action potentials (APs)] coming from the electrodes, which typically have amplitudes ranging from 10 μV to 1 mV and occupy the frequency range up to 10 kHz. Fig. 5 shows the AFE architecture, which was originally proposed in [19]. The capacitively coupled low-noise amplifier (CC-LNA) provides 40-dB gain and limits the bandwidth to 8 kHz before digitization. The amplified signal is digitized by the 10-bit, 20-kS/s asynchronous successive approximation register (SAR) analog-to-digital converter (ADC).

The CC-LNA is based on a two-stage inverter-based operational transconductance amplifier (OTA). The dc offsets on the electrodes are rejected via ac coupling, and the dc bias at the input of the OTA is set through feedback resistors constructed by diode-connected P-channel metal–oxide–semiconductor (pMOS) transistors. Although the coupling capacitors (2 pF) occupy a large area, the overall AFE maintains a small footprint due to the area savings on the ADC side.

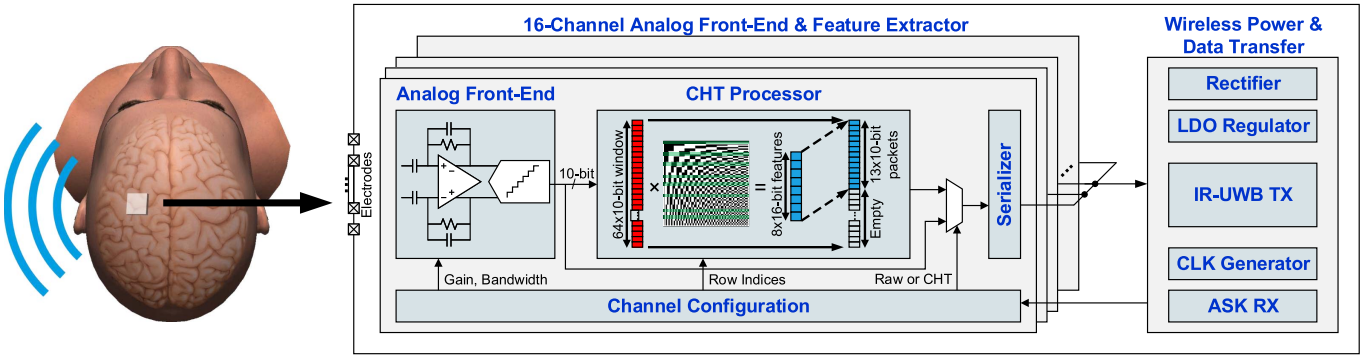


Fig. 4. Functional block diagram of the presented SoC.

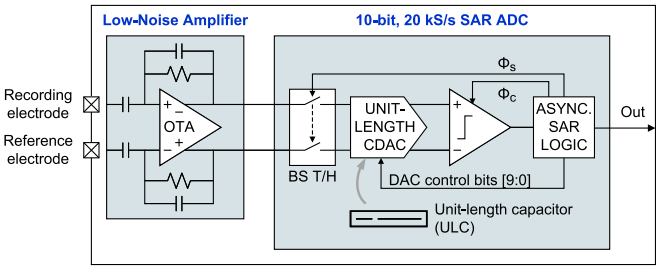


Fig. 5. Analog front-end block diagram showing the low-noise amplifier and the ADC [19].

The SAR ADC comprises a bootstrapped track-and-hold switch (BS T/H), a capacitive digital-to-analog converter (CDAC), a dynamic double-tail comparator, and an asynchronous logic circuit that implements the SAR operation. The critical block in this ADC is the CDAC. In a traditional binary-weighted capacitor array, the weights are built by replicating a unit capacitor; thus, the area of the array grows exponentially with resolution ($\propto 2^{N_B}$). The unit-length CDAC in this ADC is built using unit-length capacitors (ULCs), where the weights are set by adjusting the length difference between two differential capacitors [24]. As a result, the overall unit-length CDAC area grows linearly with resolution ($\propto N_B$). Moreover, the ULC array is constructed using higher metal layers and placed over the other active circuits with shielding in between to further reduce the footprint. These savings at the ADC side due to the unit-length CDAC results in state-of-the-art overall energy–area figure of merit (E-A FoM) with 0.78-fJ mm^2/conv. step. More details about this AFE architecture and its measurements can be found in [19].

B. CHT Processor

Fig. 6 shows the block diagram of the CHT processor and its flow of operation. The data path of the processor implements the matrix product of a 64-sample input window with eight selected rows from the 64 × 64 Hadamard matrix according to (1). Since the Hadamard coefficients are ±1, the product can be implemented by adders/subtractors instead of multipliers. 16-bit adder width is required since 64 successive additions are performed on the 10-bit ADC samples ($10 + \log(64) = 16$).

The eight rows to be computed are configured into a lookup table based on the feature importance training on the dataset. This provides power and area savings since only the patient-specific descriptive features are computed during the operation instead of the full transform. As the lookup table is populated at the start of the operation, the communication from outside to the implant does not need to be in real time.

A bank of 8 16-bit accumulators, corresponding to eight selected rows, hosts the intermediate results during the 64 cycles. Row and column counters keep track of the operation sequence. The selected row index is fetched from the configurable lookup table based on the current row counter value. The Hadamard coefficient corresponding to the selected row index and the column counter value is generated on-the-fly by a combinational logic circuit without a coefficient memory.

The clock path of the processor contains frequency dividers that generate the clocks for the ADC and the CHT processor. The master transmitter clock runs at 3.2 MHz for this 16-channel prototype for 10-bit 20-kS/s sampling. As the CHT processor computes eight features with a single shared adder/subtractor, its clock runs eight times faster than the ADC clock.

Each channel can be configured individually to output either the features computed by the CHT processor or the raw data from the AFE. When raw data are sent, the CHT processor is bypassed, and the 10-bit stream is transmitted. When features are sent, the 64-sample window reduces to a feature vector of eight features, and the bit size increases from 10 to 16 bits. To simplify the output mapping of the individually configurable channels, the 8 × 16-bit features are mapped onto a 13 × 10-bit output register, as seen in Fig. 6 (right-bottom), which is then fed into the global 10-bit data stream and sent out by the UWB transmitter.

The absence of a coefficient memory and multipliers is the main hardware advantage of the CHT over commonly used operations, such as FFT, DWT, and FIR filtering. Moreover, the transformation of the 64 × 10-bit input window into the 8 × 16-bit feature vector yields an overall data reduction of 80%. This means that five times more channels can be recorded at the same data rate with respect to raw data transmission. To illustrate, the number of channels that could be accommodated by a 40-Mb/s UWB transmitter could be increased from 200 to 1000.

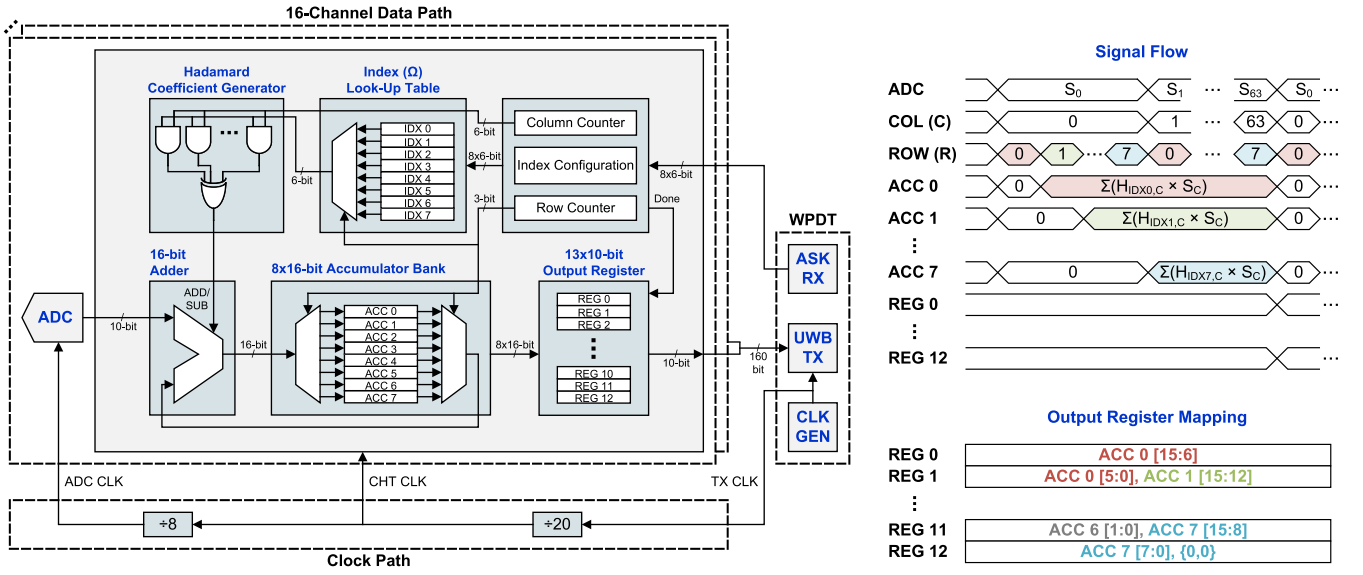


Fig. 6. Digital hardware implementation of the CHT processor, its signal flow diagram, and the output register mapping.

C. Wireless Power and Data Transfer

The on-chip power receiver blocks are shown in Fig. 7. The induced ac power on the antenna is first rectified to dc by a delay-compensated active half-wave rectifier, which is composed of a pMOS pass transistor and control circuitry. The pass transistor charges the 400-nF off-chip reservoir capacitor only when the input is higher than the output and turns off otherwise, hence the half-wave operation. The bulk of the pass transistor is dynamically biased by a composite pMOS diode to reduce the pass transistor's resistance and leakage. The timing of the switch is controlled by two comparators that detect the sign changes at the input and the output. The gate of the pass transistor is driven by a buffer stage. To improve the efficiency of the rectifier, the delays of the comparators and the gate driver are compensated by introducing offset to the comparators such that the control circuit is triggered before the input changes its sign. The rectifier is followed by a low-dropout (LDO) regulator. The regulator provides 1-V output, stabilized by a 200-nF off-chip load capacitor.

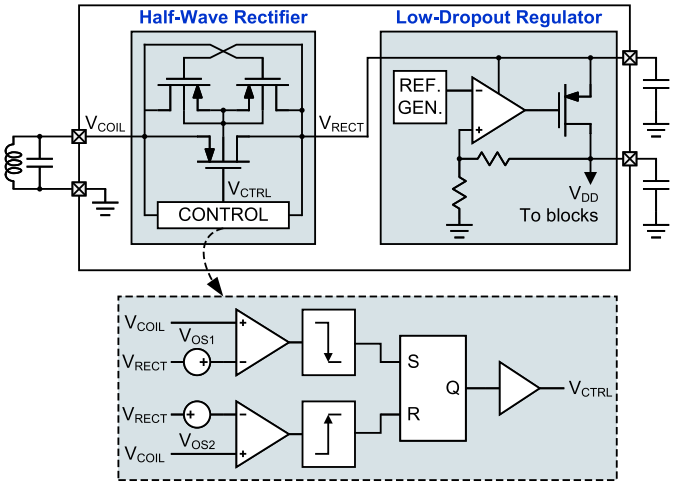


Fig. 7. Schematics of the active half-wave rectifier and the LDO regulator.

The uplink communication for this prototype is established by an impulse radio UWB (IR-UWB) transmitter. The IR-UWB pulses are generated by modulating a carrier frequency with fixed-duration pulses. The absence of a constantly-running carrier enables high energy efficiency, which makes it an attractive method for implant use. Moreover, since the standard uses a very wide bandwidth (3.1–10.6 GHz), the link is robust against deviations in center frequency due to process variation.

The schematic of the IR-UWB transmitter is drawn in Fig. 8. The 6-GHz carrier frequency is generated by an active inductor-based *LC* oscillator. The active inductor takes much less silicon area than a regular spiral inductor as it is built using only transistors (M1–M4) and resistors (R1 and R2). The pulse generator modulates the carrier frequency by driving the tail transistor (M7) of the oscillator. If the data to be sent is logic "1," the oscillator turns on for 1.8 ns mandated by the delay on the clock line. The power consumption of the transmitter is data-dependent as the oscillator turns on only for transmitting logic "1."

Fig. 9 displays the measured rectified and regulated waveforms at the output of the power receiver blocks. The power conversion efficiency of the rectifier is 71% (for 401.45-μW output power). The power supply rejection ratio of the regulator is 20 dB, and the line and load regulation values are 37.5 mV/V and 2.04 mV/mA, respectively.

Fig. 10 shows the UWB pulse characteristics in time and frequency domains. The power spectral density (PSD) of the transmitted pulses complies with the indoor emission mask regulated by the Federal Communications Commission [25]. For this 16-channel prototype, the UWB transmitter is expected to work at 3.2 Mb/s in raw data transmission mode (200 kb/s per channel) and 640 kb/s in CHT feature transmission mode (40 kb/s per channel). The maximum pulse

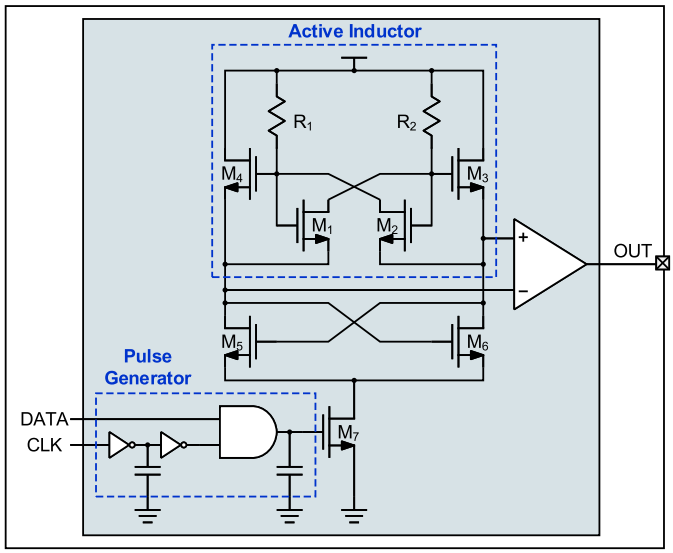


Fig. 8. Schematic of the IR-UWB transmitter.

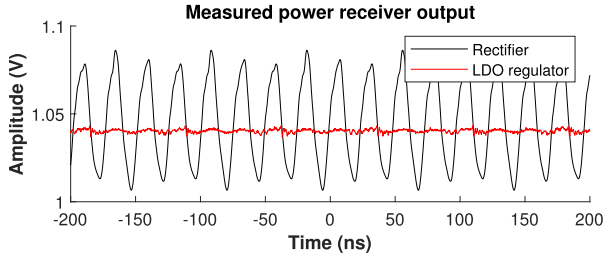


Fig. 9. Measured waveforms at the output of the power receiver blocks.

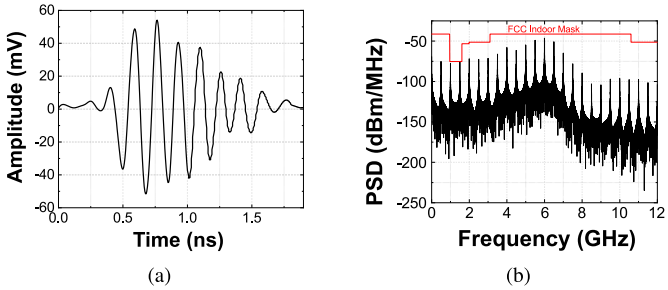
repetition frequency of the transmitter circuit was measured to be 200 MPulse/s. However, operating the wireless link at this rate would increase susceptibility to strong inter-symbol interference and result in a high bit error rate, which is the principal reason that prevents raw data transmission from 1000 channels or more. On the other hand, applying on-chip feature extraction reduces the effective data rate of the system and, thus, relaxes the link requirements.

It is important to note that the main purpose of including the WPDT subsystem in this work is to accurately compute the total power and area consumption of the proposed neural recording approach. A fully operational wireless link would require building an external UWB receiver as well, which is beyond the scope of this article. Therefore, the results presented in Section IV were obtained using a wired connection.

IV. Experimental Results

Fig. 11 displays the 16-channel prototype fabricated in TSMC 65-nm 6 × 1Z1U LP CMOS process. The dimensions, including the pad frame, are 1.6 mm × 0.78 mm, and the core blocks occupy a total of 0.382 mm^2.

Fig. 12(a) presents the area breakdown of the chip. The total area of the CHT processor is 0.121 mm^2, which is equivalent to 84k NAND2 gates in a 65-nm standard cell library. The area per channel, including the AFE and the CHT processor, is 0.021 mm^2. The total power consumption of the



(a) (b)

Fig. 10. Measured UWB pulse characteristics (a) in time and (b) frequency domains.

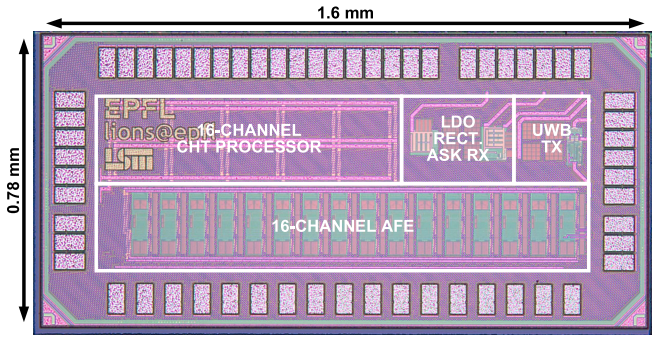


Fig. 11. Micrograph of the 16-channel wireless neural recording SoC fabricated in the TSMC 65-nm LP process.

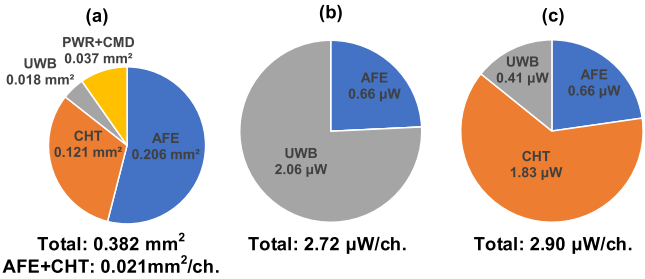


Fig. 12. Power and area breakdowns of the wireless neural recording SoC. (a) Area breakdown. (b) Power/channel (raw data). (c) Power/channel (CHT features).

chip is 401.45 μW, including the power and command receiver (355 μW). The pie charts in Fig. 12(b) and (c) show the power breakdown of the system for raw data and CHT feature transmission modes, respectively. The power consumption of the CHT processor is 1.83 μW/channel. However, the data-dependent power consumption of the UWB transmitter decreases by five times from 2.06 to 0.41 μW/channel when features are transmitted, which largely compensates for the power overhead of the feature extractor. In total, the power overhead of the CHT feature extractor is 6.7% compared to raw data transmission.

A. Waveform Reconstruction

The reconstruction mode operation was validated *in vivo* using the experimental setup shown in Fig. 13 (following all relevant ethical regulations and as approved by the Veterinary Office of the canton of Geneva (Switzerland) under license

number 32846). We used a Thy1 transgenic rat model (NBRP 0685, Kyoto, Japan), that expresses light-sensitive ion channels in the cortex. Upon illumination with a blue laser diode, pyramidal neurons are excited and create APs that can be recorded at the surface of the brain. A large craniotomy was performed, and then, a custom 16-channel soft microelectrocorticography (μECoG) array was placed epidurally over the exposed cortex. The array was microfabricated using thin-film and silicon processing technology, similar to the e-dura process [26], [27], and it was connected to the test board hosting the prototype chip using a flex cable. The test board was interfaced to a PC using a logic analyzer, where a Python script configures the chip and visualizes the recorded data in real time.

The optical stimulation was delivered using a diode-pumped solid-state blue laser (473-nm, 100-mW max power, Laserglow Technologies) coupled via an FC/PC terminal connected to a 200-μm core optical fiber (ThorLabs). Using a micromanipulator, the fiber was placed at the center of the μECoG array. The frequency and duration of the laser pulses were set as 1 Hz and 100 ms by the pulse stimulator.

The chip was configured to output first raw data and then the lowest eight Hadamard indices for reconstruction, and the outputs were reconstructed in software using a linear decoder. Fig. 14 compares the raw (top) and low-pass reconstructed (bottom) waveforms recorded at different time windows. The plots on the left correspond to the optically induced activity from all channels, and the plots on the right correspond to spontaneously captured multi-unit activities. The low-pass reconstruction discards the high-frequency components and, thus, appears smoothed.

To assess the reconstruction quality quantitatively, the prerecorded raw signals from the iEEG.org dataset [28] were fed to the CHT processor, and the outputs were reconstructed in software, as shown in Fig. 3(a). The average SNR of the low-pass reconstructed waveforms with respect to the original raw signal was found as 23 dB. This value is greater than what has been reported for random-sampling compression methods, such as compressive sensing (∼10 dB) [13], [14], [29] at similar compression ratios because the low-pass indices capture most of the energy content in neural signals.

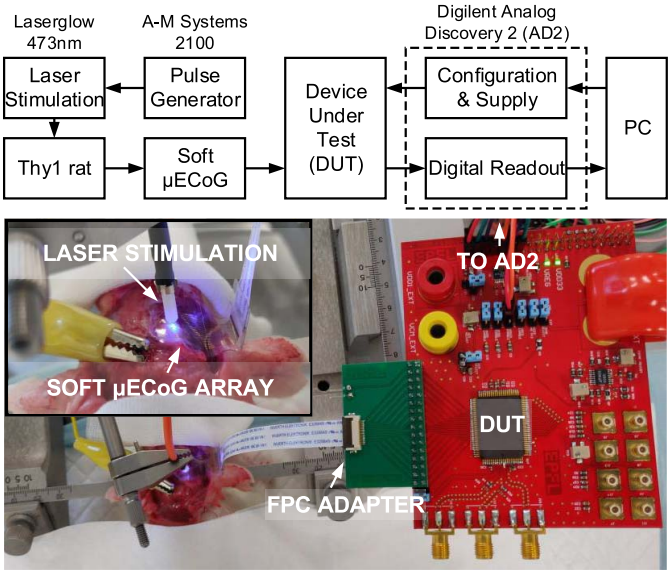


Fig. 13. Test setup for the *in vivo* validation of the reconstruction mode.

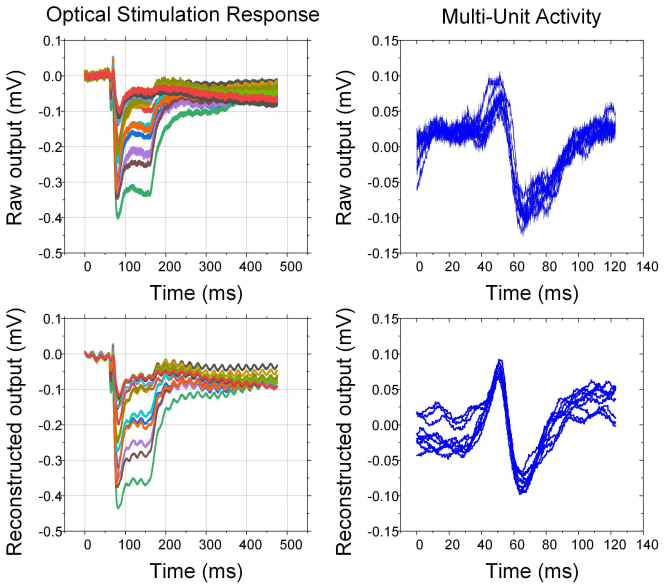


Fig. 14. Raw (top) and low-pass reconstructed (bottom) multichannel waveforms obtained during the *in vivo* experiment.

B. Epileptic Seizure Detection

Epileptic seizure detection has been a popular benchmark for neural signal classifiers due to the availability of large datasets containing hours of recordings from numerous patients. Moreover, the widespread use of spectral features for seizure detection makes it a reasonable task for demonstrating the efficacy of the proposed approach. In this work, the classification experiments were performed on two seizure datasets: CHB-MIT [30] and iEEG.org [28].

The software processing pipeline is described in Fig. 15. The raw time-series signals were first requantized to 10 bits and then reorganized into 64-sample non-overlapping windows to be compatible with the designed CHT processor. In order to standardize the different number of channels, initial training was performed to select the most descriptive 16 channels per patient and eight Hadamard indices per channel. The learned indices and the raw data from the learned channels are then fed to the CHT hardware, whose output is processed by the off-chip classifier.

The classifier was implemented in software as an ensemble of eight binary decision trees with a maximum depth of 4. A binary decision tree compares the input feature vector with a series of thresholds to output a probability. The tree ensemble produces the final decision as the weighted sum of the different tree outputs to accommodate variability in the data. The training of this model was done in Python language using the XGBoost package [31]. A new model was trained for each study to avoid underfitting due to the large patient-to-patient variations. The patient data were partitioned into

TABLE I
COMPARISON WITH THE STATE OF THE ART

	TBCAS'16 [14]	JSSC'17 [10]	JSSC'18 [17]	JSSC'20 [22]	ISSCC'18 [18]	**This work**
Technology	180 nm	130 nm	130 nm	40 nm	180 nm	**65 nm**
V_{DD} [V]	1.8**	1.2	1.2	0.58	1.5	**1**
Number of Channels	16	64	32	14	8	**16**
Blocks Included	AFE+COMP+TX	AFE+FE+CLF+TX	AFE+FE+CLF	FE+CLF	AFE+FE+CLF	**AFE+FE+TX**
Total Area [mm^2]	1.68	3.86	7.59	2.56	5.83	**0.382**
Total Power [mW]	0.254	0.47*	0.714**	1.9	0.013**	**0.0464***
Feature Extractor / Compressor	CS	FIR+PLV	FIR+PLV/SE/CFC	FFT+SE	DWT+KDE	**CHT**
Waveform Reconstruction	Yes	No	No	No	No	**Yes**
Compression Ratio	8	-	-	-	-	**5**‡‡
Reconstruction SNR [dB]	9.78	-	-	-	-	**23**
Compressor power [μW/channel]	4.81	-	-	-	-	**1.83**
Compressor area [mm^2/channel]	0.015‡	-	-	-	-	**0.0076**
Dimensionality Reduction	-	-	Autoencoder	mRMR	ICA	**XGBoost**
Feature Dimension	-	n/r	125	16	48	**128**
Feature Computation	-	Fixed	Fixed	Fixed	Fixed	**Adaptive**
Feature Extractor Area [mm^2]	-	1.285	0.475‡	0.618‡	0.817‡	**0.121**
Classification Rate [class/s]	-	n/r	4	11.1	0.074	**312.5**
Energy/Classification [μJ]	-	n/r	168.6	170.9	14.2	**0.149**†
Classifier Algorithm	-	Threshold	SVM	SVM	SVM	**XGBoost DT**
Dataset	-	Custom	EU	CHB-MIT	CHB-MIT	**CHB-MIT**
Sensitivity	-	75%	100%	96.6%	97.8%	**97.8%**††
False Alarm Rate/Specificity	-	0.5/h	0.81/h	0.28/h	99.7%	**0.12/h**††

* Power management blocks excluded. ** Estimated from the reported values. ‡ Estimated from the micrograph.
‡‡ Effective ratio including the bit width increase. † Total energy for AFE, FE and TX combined. †† Off-chip classifier.

sequences where each sequence was at least 1 h long and contains at least one seizure. The sequences were then split into training and test sets for leave-one-out cross-validation.

Although the lowest indices carry most of the energy in the raw signal, as discussed in Section II, Fig. 16 shows that the higher indices contain significantly more information for seizure classification. For the CHB-MIT dataset, the index ranges of 15–20 and 40–45 have significantly higher importance. If we relate these indices to frequencies with 256-S/s sampling rate, they correspond to 30–40- (low-γ) and 80–90-Hz (γ) bands, respectively. For the iEEG.org dataset, the important index ranges are 5–15, 28–30, and 57–64, which correspond to 20–60- (low-γ), 110–120- (high-γ), and 220–250-Hz (ripple) bands, respectively, with a 500-S/s sampling rate. These findings are in accordance with the epilepsy literature, suggesting the utility of high-frequency oscillations (HFOs) for seizure detection [32]. In most threshold-based compression methods, these components would be discarded as they carry little energy and do not contribute to achieving a high post-reconstruction SNR. Training finds the most descriptive indices per patient, which leads to a high sensitivity rate.

Fig. 17 presents the results obtained for each study in the two datasets containing a total of 283 seizures from 40 patients. For most patients, all seizures could be detected with no false alarms. The average sensitivity for the CHB-MIT dataset was 92% and reaches 97.8% if the two outliers (chb06 and chb16) are excluded. The false alarm rate (FAR) is 0.117/h, which corresponds to around three false alarms per day. The average sensitivity for the iEEG.org dataset is 90.5%, and the FAR is 0.171/h, corresponding to around four false alarms per day.

C. SD Detection

SDs are pathological electrical waves propagating at the surface of the cortex, which is observed in a number of illnesses, such as traumatic brain injury or stroke. Their presence reveals metabolic and electrical instability of the brain and serves as a direct measure of neuronal health and potential ongoing lesion growth [33]. Although SDs monitoring could serve as a critical diagnostic tool in the intensive care unit, it is rarely exploited in clinics in part because of the difficulty of monitoring the multichannel data continuously by clinicians, as it is currently done with six-contact electrode strips [33], [34]. Therefore, methods to extract and transmit large-scale information from multichannel data to automated SD detection algorithms are of high interest.

To test the applicability of the proposed CHT approach for identifying SDs in large-scale recordings, we performed an *in vivo* experiment where SD was chemically induced through topical applications of potassium chloride (following all relevant ethical regulations and as approved by the Veterinary Office of the canton of Geneva (Switzerland) under license number 33223). The raw data were prerecorded using a soft electrode array (3 × 3 grid of 500-μm-diameter electrodes [27]) connected to a wireless recording system (Multi

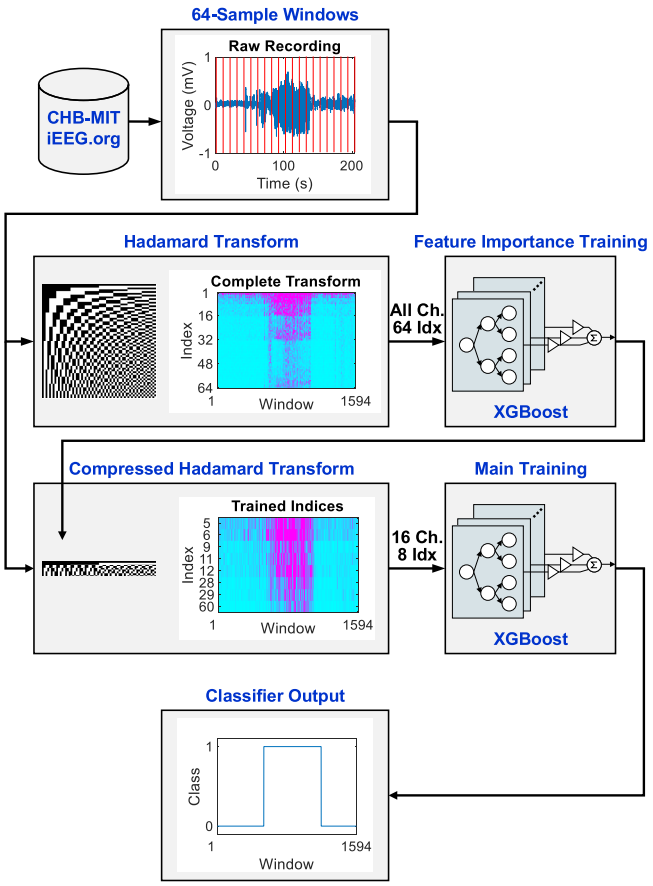


Fig. 15. Processing pipeline of the classification experiments.

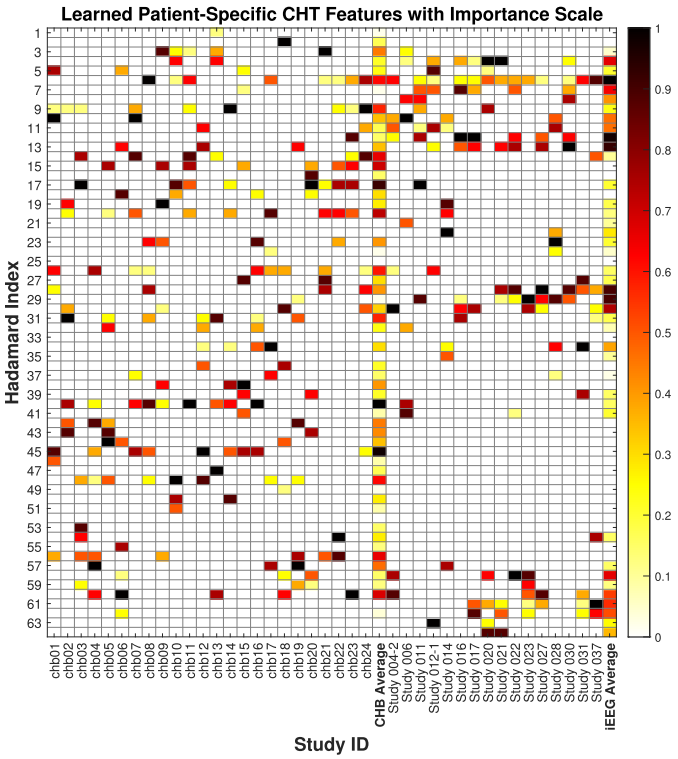


Fig. 16. Learned CHT indices for each study in the CHB-MIT and iEEG.org datasets. The color bar indicates the importance scale of the eight selected indices out of 64.

CHB-MIT Dataset					iEEG.org Dataset				
Study ID	# Seiz.	# Det.	Sensitivity	FAR	Study ID	# Seiz.	# Det.	Sensitivity	FAR
chb01	7	7	100%	0.143/h	Study 004-2	3	3	100%	0.000/h
chb02	3	3	100%	0.000/h	Study 006	4	2	50%	0.125/h
chb03	7	7	100%	0.140/h	Study 011	3	3	100%	0.000/h
chb04	4	4	100%	0.667/h	Study 012-1	6	4	67%	0.250/h
chb05	5	5	100%	0.000/h	Study 014	8	7	88%	0.000/h
chb07	3	3	100%	0.000/h	Study 016	7	7	100%	0.714/h
chb08	5	5	100%	0.000/h	Study 017	9	9	100%	0.000/h
chb09	4	4	100%	0.333/h	Study 020	8	7	88%	0.438/h
chb10	7	7	100%	0.000/h	Study 021	9	8	89%	0.722/h
chb11	3	3	100%	0.000/h	Study 022	7	7	100%	0.000/h
chb12	27	26	96%	0.000/h	Study 023	4	4	100%	0.250/h
chb13	10	9	90%	0.286/h	Study 027	6	6	100%	0.000/h
chb14	8	8	100%	0.000/h	Study 028	9	6	67%	0.111/h
chb15	20	20	100%	0.000/h	Study 030	8	8	100%	0.063/h
chb17	3	3	100%	0.667/h	Study 031	4	4	100%	0.000/h
chb18	5	5	100%	0.000/h	Study 037	8	8	100%	0.063/h
chb19	3	3	100%	0.000/h	Total	103	93	90.5%	0.171/h
chb20	8	8	100%	0.000/h					
chb21	4	4	100%	0.000/h					
chb22	3	3	100%	0.000/h					
chb23	7	5	71%	0.333/h					
chb24	16	15	94%	0.000/h					
chb06	10	2	20%	0.000/h					
chb16	8	3	38%	0.400/h					
Total	162	157	97.8%	0.117/h					

Fig. 17. Summary of the classification results on the CHB-MIT and iEEG.org datasets.

Channel Systems W2100, 0.01-Hz high-pass filter, and 2-kHz sampling rate). The subsequent processing was performed on the CHT hardware.

The raw recorded brain signal on one electrode (sampled at 2 kHz) is shown in Fig. 18 (top), as well as its complete HT (center) and its CHT (bottom). The complete 64 × 64 HT enables the systematic detection of the SD waves characteristics (increased low-frequency activity and decreased high-frequency activity). The proposed CHT approach captures the information content with only eight indices.

D. Discussion

Table I summarizes the performance of the presented neural recording SoC and compares it with previous works implementing on-chip compression [14] and classification [10], [17], [18], [22]. The proposed on-chip feature extraction approach has several advantages. First, the CHT processor occupies only 0.121 mm^2 for 16 channels, which is much less than the conventional feature extractors based on FFT, DWT, and FIR filters. Second, this work computes only the most descriptive features that are identified and configured by the learning algorithm, instead of applying dimensionality reduction on all computed features. As a result, the output data rate could be reduced by five times while achieving a similar seizure detection performance. Third, the CHT features allow waveform reconstruction on the receiver side for monitoring or further post-processing. The process-normalized hardware efficiency of CHT is similar to a multiplierless and memoryless CS [14] implementation with higher reconstruction quality at a similar compression rate. Finally, the combined energy cost of sensing (AFE), processing, (CHT), and transmitting UWB per feature vector (0.149 μJ) is much less than the cost of an on-chip classifier. Therefore, the proposed approach makes it feasible to send multichannel data to off-chip, more advanced, and flexible classifiers.

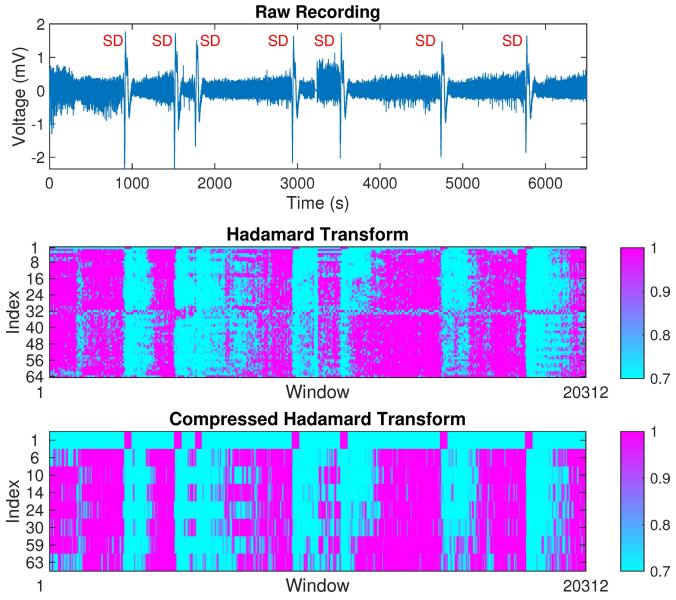


Fig. 18. Dimensionality reduction using CHT of cortical activity from one electrode containing induced SDs.

V. Conclusion

Future neural recording systems have to be fully implantable and operated wirelessly to decrease infection risks and increase patient independence. Nevertheless, the data throughput requirement of massively parallel recordings cannot be met with current wireless solutions for implants. In this article, we presented a neural recording SoC with on-chip feature extraction capability to tackle the data rate bottleneck. The chip extracts spectral features on-chip using versatile and hardware-friendly CHT, which are then sent out to an off-chip classifier to maintain algorithm flexibility. This configuration not only relaxes the hardware constraints but also enables versatility for facilitating different classification purposes. The selection of the features to be sent out is driven by the feature importance training of the off-chip classifier, which ensures that only relevant information is transmitted. As a result, the transmitted data rate is reduced by 80% without compromising the detection performance. The second mode of operation for the CHT feature extractor is waveform reconstruction, which can be used for algorithm calibration, clinical research, and debugging. The 16-channel prototype in 65-nm CMOS containing the AFE, the CHT processor, and the WPDT subsystem achieves 2.9-μW power and 0.021-mm^2 area per channel. These results would enable massively parallel neural recording systems even with strict resource limitations. For example, a 1000-channel system would be feasible within a single 4 mm $\times$ 5 mm chip with 2.9-mW power consumption and 40-Mb/s data rate using the proposed approach.

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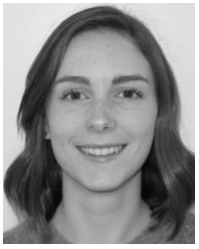

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