17.2 A 2.4pJ/b 100Gb/s 3D-Integrated PAM-4 Optical Transmitter with Segmented SiP MOSCAP Modulators and a 2-Channel 28nm CMOS Driver

Arian Hashemi Talkhooncheh[1], Weiwei Zhang[2], Minwo Wang[1], David J. Thomson[2], Martin Ebert[2], Li Ke[2], Graham T. Reed[2], Azita Emami[1]

[1]California Institute of Technology, Pasadena, CA
[2]University of Southampton, Southampton, United Kingdom

Data centers continue to require interconnects with higher bandwidth densities and energy efficiencies. Silicon photonics (SiP)-based solutions have gained interest for implementing low-cost and power efficient 100+Gb/s/λ optical transceivers. While microring modulators (MRMs) have small footprints and high electro-optical bandwidth (EOBW), they suffer from an inherent tradeoff between bandwidth and optical phase efficiency, high sensitivity to process and temperature variations, and non-linear electro-optic characteristics [1-2]. Travelling-wave Mach-Zehnder Modulators (TW-MZMs) require power-hungry drivers to compensate microwave losses and occupy large areas on chip [3-4]. Metal-oxide-silicon-capacitor (MOSCAP)-based phase modulators can significantly scale the area and power of the optical transmitter (OTX) owing to their superior optical efficiency (voltage-length product at π phase shift of $V_\pi L < 1V{\cdot}mm$) and compact footprint (< 1mm) [5]. MOSCAP modulators, however, impose large capacitive parasitics (~3fF/μm), which could limit the electro-optical bandwidth (EOBW) significantly. State-of-the-art wireline transmitters cannot meet the requirements of MOSCAP modulators due to their 50Ω-terminated design and limited output voltage swing [6]. This paper presents a 3D-integrated 100Gb/s PAM-4 OTX with electronic pre-distortion (PD) and BW extension techniques to compensate for MOSCAP modulator BW limitations.

A system-level block diagram of the OTX is shown in Fig. 17.2.1. It consists of a silicon-photonic IC (PIC) and a CMOS electronic IC (EIC) flip-chip-bonded together using gold micro-pillars. The PIC consists of a segmented push-pull MZM with MOSCAP phase modulators, thermal phase shifters on each arm for relative phase adjustment, and grating couplers for optical I/O. The MOSCAP phase modulators consist of a MOS junction using p-type doped silicon and an SiO_2 slot along the Si waveguide, which can introduce a high-speed optical refractive index change in accumulation mode. The details of the parasitic structure of the MOSCAP modulators are depicted in Fig. 17.2.1. The lengths of the MOSCAP modulator segments are optimized to take advantage of their optical modulation efficiency ($V_\pi L$) with nominal supply voltages of the 28nm CMOS process (0.9V) to minimize the EIC power consumption. The co-optimization of PIC and EIC resulted in MOSCAP segment lengths of 450μm (MSB) and 170μm (LSB) with estimated parasitic capacitances of 500fF (LSB) and 1pF (MSB). The MSB modulator segments are U-shaped to effectively double modulation efficiency with a fixed electrode length of 150μm, and to avoid travelling-wave reflection effects, which require power-hungry terminations. The EIC includes two channels of 50Gb/s NRZ TX with differential outputs, a 25GHz clock buffer that amplifies the external clock signal to drive on-chip serializers, and a look-up-table (LUT)-based control unit to configure the driver peaking, pre-distortion settings and the timing between the two driver data paths.

The top-level block diagram of the EIC is provided in Fig. 17.2.2. Each driver receives two pairs of independent 25Gb/s differential data inputs, which are buffered through a CML-to-CMOS stage. A 25GHz differential input clock is buffered and adjusted for its duty cycle internally before driving the serializers. For each driver slice, the 25Gb/s data streams are combined on chip through a 2-to-1 serializer using the 25GHz clock signal. An LUT-based delay control unit fine-tunes the relative clock delays between the serializers. Another delay adjustment unit is placed after the serializers to calibrate the 50Gb/s data delay between the driver slices. Active peaking is used in the data buffers both at the back-end and the 50Gb/s buffering stage. The two 50Gb/s data streams are delivered to the last stage drivers. Each current-mode differential driver is BW-optimized for the corresponding MOSCAP segments with similar lengths on each of the MZM arms. A reconfigurable pre-distortion block generates current pulses with tunable widths at each data transition to further improve the effective driver BW.

The schematics of the data stream delay generators, pre-distortion pulse-width control and driver cores are depicted in Fig. 17.2.3. Digitally controllable current-starved stages are used to fine-tune the relative delay between the differential data paths in each slice, as well as the phase difference between the two slices. Cross-coupled active peaking is repeatedly used to improve the limited data transition times (from 12ps to 8ps) and to minimize ISI. The active peaking is achieved by resistive-feedback inverters with adjustable feedback resistors and cross-coupled inverter pairs. The 50Gb/s data streams are further buffered through two separate paths. The main path consists of fixed-size buffers that deliver the data to both the driver core and the pre-distortion block. The 2nd path includes a digitally controllable delay generator in addition to buffers using bypassing inverter stages. The data stream from the 2nd path is also sent to the pre-distortion block, which generates current pulses with adjustable widths (2ps, 4ps or 6ps) based on the chosen delay. The LSB driver core (final stage) is a CML differential pair with differential T-coil peaking and reconfigurable load resistors. Two 100fF cross-coupled capacitors are placed at the input of the LSB core driver to further increase the BW. The same architecture is used for the MSB driver core with differential shunt peaking and 2× stronger pre-distortion drivers to drive 1pF loads at each output node.

At the driver back-end, a CML-to-CMOS stage with differential active peaking, shown in Fig. 17.2.4, is used to amplify the incoming data streams at each data input. The external 25GHz clock is amplified by a CML-to-CMOS stage and then passed through AC-coupled inverter-based TIA stages and buffers. The clock duty cycle is adjusted by a duty-cycle-correction (DCC) block, which uses controlled DC current injection to adjust the transition times. The two 25Gb/s data streams and the 25GHz clock are then delivered to the 2-to-1 serializer. The serializer is a differential mixer followed by a CML-to-CMOS stage and differential active peaking block to generate clean 50Gb/s streams.

The TX EIC is fabricated in a 28nm CMOS process with an active area of ~0.2mm², which measures 830μm by 750μm. The segmented push-pull MZM is implemented on the PIC with an overall footprint of ~1mm². All control signals, voltage supplies (0.9V) and the current reference were delivered to a test PCB, on which the 3D-integrated OTX was mounted. An external arbitrary waveform generator (AWG) provides 25Gb/s PRBS-31 data streams, a 25GHz clock signal to the EIC, and a trigger signal for an optical sampling scope (OSS). The modulated optical output is fiber-coupled to the OSS receiver for eye diagram recording and TX dispersion eye closure (TDEC and TDECQ) measurements. An external laser source inputs 10dBm optical power at 1550nm to the PIC via a grating coupler. The fiber-to-chip coupling losses are estimated to be 4.5~5.5dB/port. An erbium-doped fiber amplifier (EDFA) is placed after the OTX to amplify the optical signals by 11dB before the OSS. Considering a trade-off between the optical efficiency ($V_\pi L$) and the EOBW of the MOSCAP modulators when their bias voltage is increased, all segments were forward biased at 1V for optimal performance.

The 50Gb/s NRZ and 100Gb/s PAM-4 optical eye measurements are shown in Fig. 17.2.5. The top row shows the eye diagrams when minimum peaking and minimum pre-distortion settings are applied. The 2nd row shows the measured raw eye diagrams using the optimal BW extension settings for the driver. The measured OMA (including coupling and on-chip insertion losses as well as the EDFA gain) was 1.4dBm. Both eye diagrams were filtered by IEEE 802.3bs compliant 5-tap equalizers, shown on the 3rd row of Fig. 17.2.5, to measure a TDEC of 0.76dB and TDECQ of 1.53dB. A stand-alone EOBW measurement of 200μm and 400μm MOSCAP modulators, using a 65GHz 50Ω terminated probe, shows 16GHz and 23GHz BW at 1V forward bias, which are provided in Fig. 17.2.6. These measured BWs are significantly below the required BW for 50Gbaud modulation, which further highlights the effectiveness of the reconfigurable on-chip pre-predistortion and peaking in improving the eye quality.

The EIC dissipates 240mW at 100Gb/s PAM-4 (including clock distribution, serializers and core drivers) to deliver 4dB total ER at 1.53dB TDECQ. The power breakdown of the EIC components, as well as the OTX performance summary are provided in Fig. 17.2.6. The proposed TX achieves 2.5× better EIC energy efficiency at 100Gb/s, compared to the state-of-the-art co-integrated optical PAM-4 transmitters. The PIC exhibits an overall 6.2dB of optical insertion loss (including the 3dB quadrature point loss). The proposed tightly integrated SiP-CMOS OTX demonstrates the potential of compact MOSCAP modulators co-optimized with CMOS drivers, to provide a path for 100+Gb/s/λ SiP transmitters.

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References:
[1] H. Li et al., "A 112 Gb/s PAM4 Silicon Photonics Transmitter With Microring Modulator and CMOS Driver," *IEEE Journal of Lightwave Technology*, vol. 38, no. 1, pp. 131-138, Jan. 2020.
[2] H. Li et al., "A 3-D-Integrated Silicon Photonic Microring-Based 112-Gb/s PAM-4 Transmitter With Nonlinear Equalization and Thermal Control," *IEEE JSSC*, vol. 56, no. 1, pp. 19-29, Jan. 2021
[3] E. Sentieri et al., "A 4-Channel 200Gb/s PAM-4 BiCMOS Transceiver with Silicon Photonics Front-Ends for Gigabit Ethernet Applications," *ISSCC*, pp. 210-212, Feb. 2020.
[4] K. Li et al., "Electronic–photonic convergence for silicon photonics transmitters beyond 100 Gbps on–off keying," Optica 7, 1514-1516 (2020).
[5] T. Hiraki et al. "Heterogeneously integrated III–V/Si MOS capacitor Mach–Zehnder modulator," Nature Photon 11, 482–485 (2017).
[6] M. Choi et al., "8 An Output-Bandwidth-Optimized 200Gb/s PAM-4 100Gb/s NRZ Transmitter with 5-Tap FFE in 28nm CMOS," ISSCC, pp. 128-130, Feb. 2021.

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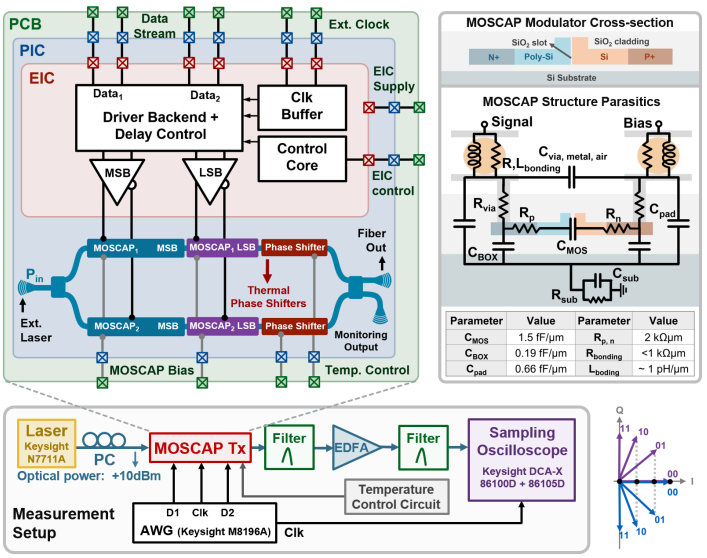


Figure 17.2.1: Top-level block diagram and measurement setup of the optical PAM-4 transmitter. MOSCAP modulator cross-section and parasitics.

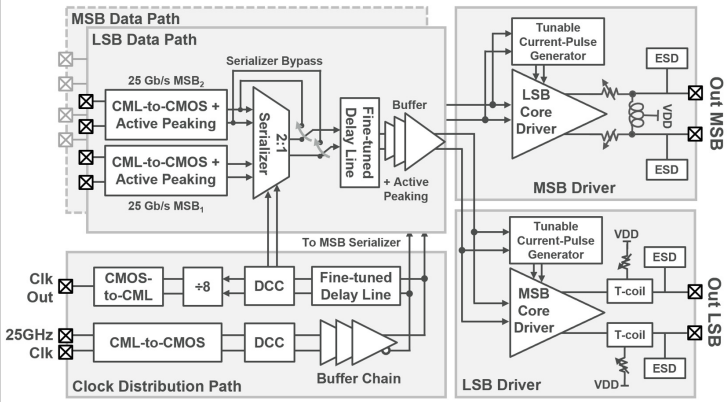


Figure 17.2.2: Top-level block diagram of the 2-channel CMOS driver.

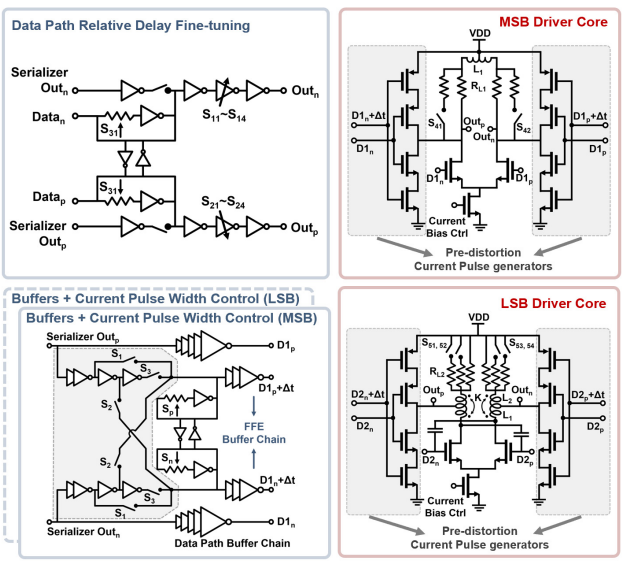


Figure 17.2.3: Tunable data delay generator, data-path buffers, current pulse-width control and driver core circuitry.

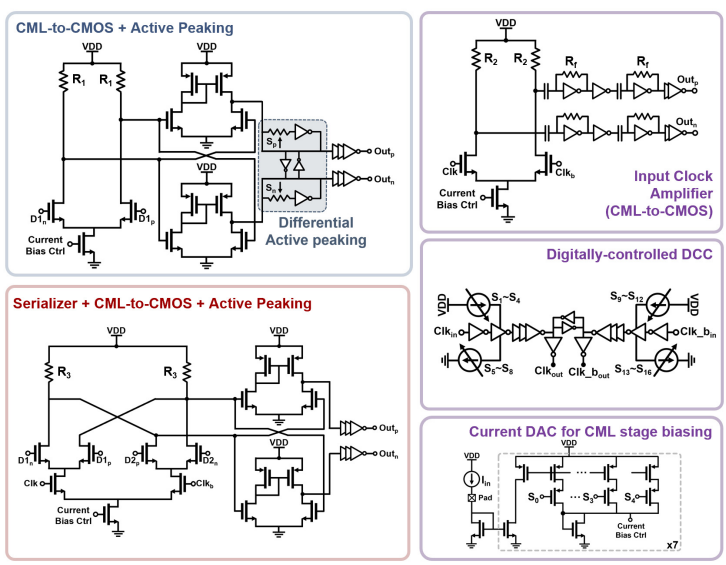


Figure 17.2.4: Drivers back-end, serializer, clock buffer, DCC and bias control circuitry.

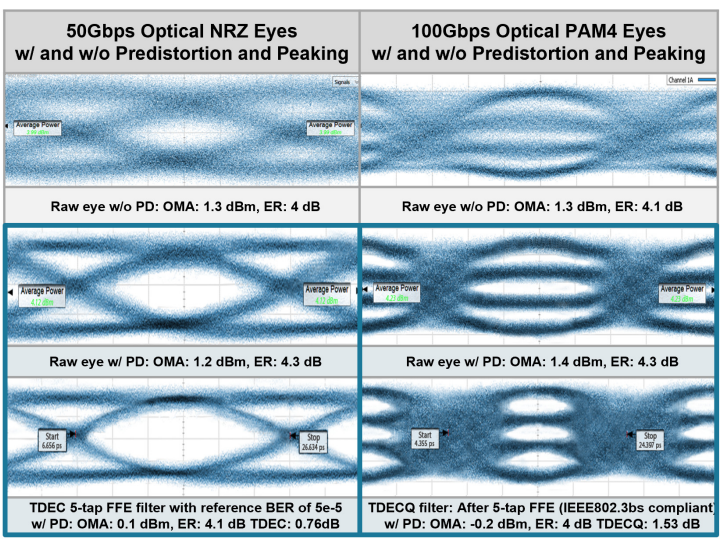
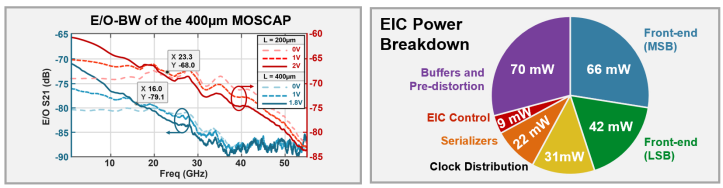


Figure 17.2.5: Measured 50Gb/s NRZ and 100 Gb/s PAM-4 eye diagrams before and after on-chip BW extension.



Comparison Table	[1] JLT'20	[2] ISSCC'20	[3] ISSCC'20	This Work	
Technology	28nm CMOS	28nm CMOS	55nm BiCMOS	28nm CMOS	
Integration	Wire-bond	3D	3D	3D	
Modulation Device	MRM	MRM	TW-MZM (6mm)	Lumped-MZM (620µm)	
Operating Wavelength	1310 nm	1310 nm	1310 nm	1550 nm	
Output Voltage Swing	3 V_{ppd}	3 V_{ppd}	3.6 V_{ppd}	1.2 V_{ppd}	
FFE / Pre-distortion	NL FFE + PD	NL-FFE + PD	No	Reconfigurable PD	
Signaling	PAM4	PAM4	PAM4	NRZ	PAM4
Data Rate (Gb/s)	112 Gb/s	112 Gb/s	53.15 Gb/s	50 Gb/s	100Gb/s
Total Optical OMA	-1.24 dBm	-5.2 dBm	0.4 dBm	1.2 dBm [1]	1.4 dBm [1]
TDECQ	0.5 dB	0.88 dB	1.8 dB	0.76 dB	1.53 dB
Input Laser Power	13 dBm	12 dBm [2]	13.5 dBm	10 dBm	
Chip Active area (mm²)	N/A	2.25 [3]	44	0.62	
EIC Power Efficiency (pJ/bit)	6	6	5.2	2.4 [4]	

1: Including coupling losses, on-chip IL and EDFA gain
2: Estimated from total laser power of 160mW
3: Active area is 0.4mm²
4: Including serializers, clock path and control

Figure 17.2.6: Measured E/O BW of MOSCAP modulators for various biases, EIC power breakdown. Performance summary and comparison to prior art.

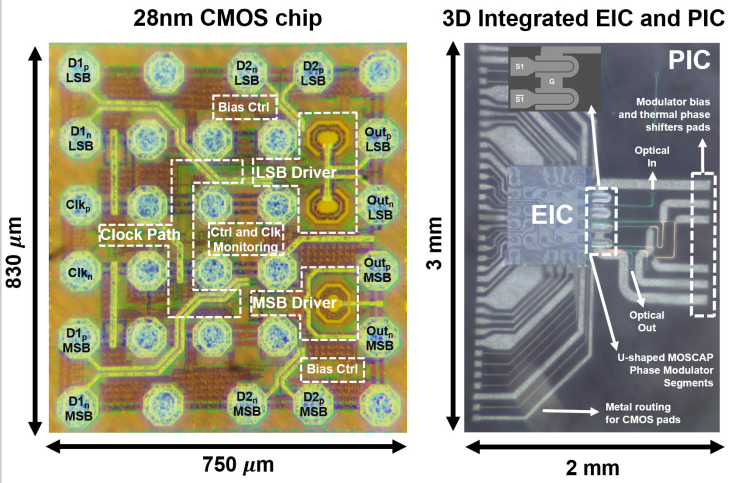


Figure 17.2.7: 28nm CMOS Chip Micrograph and the 3D-integration with the PIC.

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