Nonlinear Equalization for Optical Interconnects

Kuan-Chang Chen and Azita Emami
Department of Electrical Engineering, California Institute of Technology, Pasadena, CA, USA, kcxchen@caltech.edu

***Abstract*—This paper focuses on nonlinearity compensation schemes for optical interconnects. Receiver-side digital nonlinear equalizers are investigated, and a custom piecewise-linear equalizer is proposed as an energy-efficient candidate. Transmitter-side techniques utilizing nonlinear electrical drivers or segmented optical modulators are reviewed.**

Keywords—PAM4, modulator, nonlinear, equalization, electrical, optical, interconnect, digital signal processing

I. Introduction

Optical interconnects have demonstrated advantages in supporting high-speed and long-distance data communication with better energy efficiency, in contrast to the electrical counterparts restrained by the frequency-dependent losses of the channel. To address the ever-growing data traffic, the use of high-order modulation formats shows attractive potential, by enabling greater spectral efficiency and thus higher data rates. However, dividing the peak modulation amplitude into multiple levels, in consequence of adopting a high-order modulation format, results in a more stringent signal-to-noise ratio (SNR). In optical interconnects, the nonlinearity stemming from the modulators can further detrimentally compromise the eye-opening, as it causes mismatched level-separations and/or dynamics. Hence, nonlinearity compensation, or nonlinear equalization, holds the key to realizing the greater data bandwidth empowered by high-order-modulated optical interconnects. In this paper, transmitter- and receiver-side nonlinear equalization techniques, including our proposed learning-based digital piecewise-linear (PWL) equalizer, are presented.

II. Receiver-Side Digital Equalization

Receiver-side equalization techniques can compensate for the accumulated signal impairments including those arising from the channel or the receiver front-end circuits, whereas transmitter-side equalization would require a back-channel to capture the overall signal characteristics. Moreover, when an analog-to-digital converter is included in the receiver, equalization can be implemented in the digital domain, which holds strong immunity against process, voltage, and temperature (PVT) variations and benefits from the CMOS technology scaling. In this article, we show that the symbol-error-rate (SER) can be improved by receiver-side digital nonlinear equalizers, and that power consumption can be saved by replacing the relatively power-hungry multipliers (MULs) with adders (ADDs). Fig. 1(a) shows a representative example of the simulated normalized PAM4 eye-diagram and sample constellations of a micro-ring-modulator (MRM)-based transmitter modeled in [1]. This MRM is driven by a linear PAM4 driver at 50 Gb/s, and as shown in Fig. 1(a), nonlinearities in the forms of mismatched level-separations and dynamics are observed in its outputs. Volterra series fitting is applied on the sample constellations, which reveals the most prominent nonlinear terms are the second-order products of the current data symbol (D_K) and the previous data symbol (D_{K-1}). Accordingly, nonlinear equalizers can focus on compensating for the D_K^2, $D_K D_{K-1}$, and D_{K-1}^2 terms. Fig. 1(b) presents one conventional solution, which integrates a second-order Volterra equalizer of memory length 2 with a 5-tap linear feedforward equalizer (FFE). Fig. 1(c) shows our proposed equalizer employing a custom PWL function, full-wave rectified linear unit (FReLU). The FReLU is defined with two learnable parameters, p and q, as shown in the inset of Fig. 1(c). The FReLU plays the central role in generating approximations for the second-order terms, as its shape roughly resembles that of a quadratic function. Referring to Fig. 1(c), the output of linear FFE (i.e., L_K) extracts data information of ($D_K + \alpha D_{K-1}$) from the received samples; consequently, the output of FReLU (i.e., A_K) contains the information of $(D_K + \alpha D_{K-1})^2$, where α depends on the nonlinearity characteristics. The (αD_{K-1}) and $(\alpha D_{K-1})^2$ terms in L_K and A_K can be varied or compensated, by weighted-summing the L_{K-1} and A_{K-1} terms reused from precedent computations, at the cost of one extra MUL and one extra ADD for each. The equalizers shown in Fig. 1(b) and Fig. 1(c) are referred as VT-FFE and PWL-FFE, respectively. To study the SER performance of VT-FFE and PWL-FFE, a statistical method is developed for computing the approximate cumulative distribution function (CDF) and the complementary CDF of the nonlinearly filtered noise at each signal level. In the SER computations, only the equalizer architecture is altered, while the other link configurations are kept identical. Fig. 1(d) reports the SER performance and the hardware overheads of the nonlinear equalizers. The conventional VT-FFE and the proposed PWL-FFE lead to similar improvements in SER,

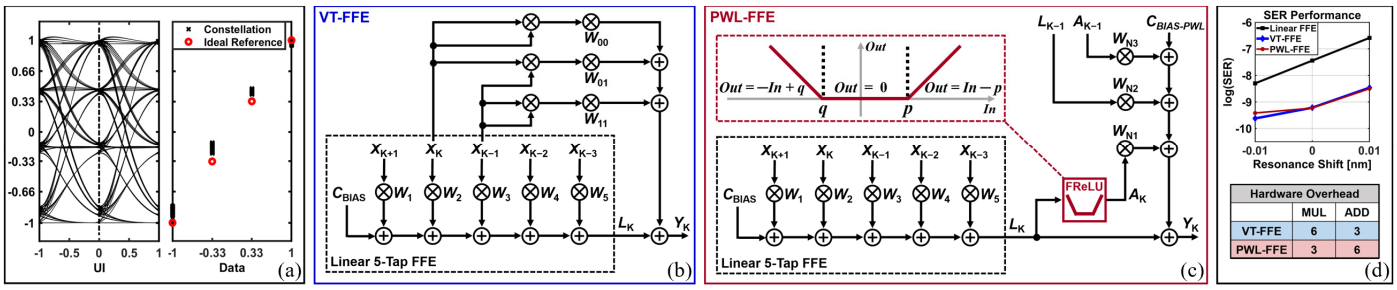

Fig. 1. (a) Simulated PAM4 eye-diagram and signal constellations at 50 Gb/s. (b) Volterra equalizer of memory length 2 with 5-tap linear FFE (VT-FFE). (c) Proposed PWL nonlinear equalizer with 5-tap linear FFE (PWL-FFE). (d) SER performance and the nonlinear equalizer hardware overhead.

978-1-6654-1601-6/21/$31.00 ©2021 IEEE

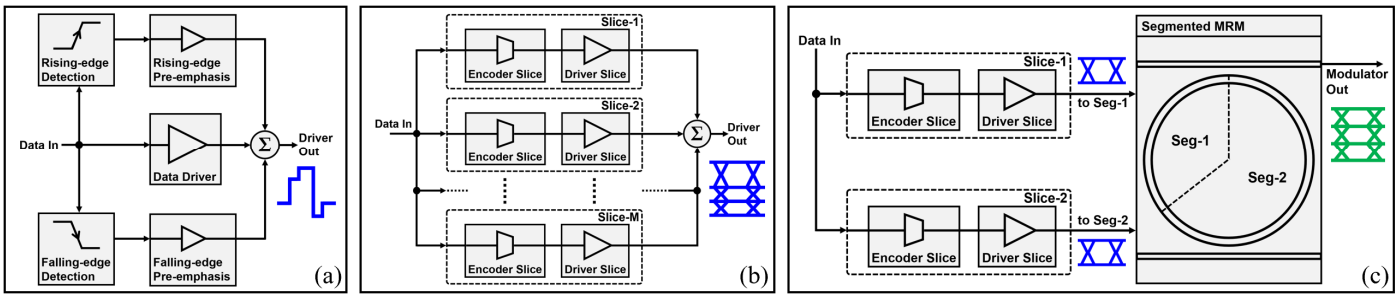

Fig. 2. Transmitter-side nonlinear equalization concepts. (a) Electrical driver embedded with asymmetrical pre-emphasis [2]. (b) Segmented electrical driver as an electrical DAC for pre-distortion/emphasis [3]. (c) Segmented optical modulator as an optical DAC, with its driver circuits. A two-segment example is shown [4].

with or without the MRM resonance shifts up to ±0.01 nm. However, PWL-FFE requires only half of the MUL overhead in VT-FFE, by employing more ADDs (including the 2 ADDs in implementing FReLU). Synthesized with 12-bit resolution in a commercial 28-nm CMOS technology, the proposed PWL-FFE favorably consumes 37% less power overhead in comparison with VT-FFE.

III. Transmitter-Side Equalization

The transmitter-side nonlinear equalization aims to enlarge and equalize the eye-openings for achieving better link SER performance. The pivotal transmitter-side equalization techniques are described in this section with examples. In [2], a vertical-cavity surface-emitting laser (VCSEL)-based NRZ transmitter is modeled, where input data bit 1 and bit 0 give rise to asymmetrical output pulse responses, attributed to the uneven reactions to the rising and falling edges of modulation. The solution proposed in [2] is shown in Fig. 2(a), which detects the rising and falling edges and correspondingly applies different amounts of pre-emphasis to mitigate the asymmetry. This technique improves the eye-opening and meanwhile ameliorates the transmitter energy efficiency by allowing the VCSEL to be driven at lower bias currents [2]. The foregoing suggests that with the inclusion of two auxiliary paths for asymmetrical pre-emphasis, the nonlinear modulation dynamics in NRZ systems can be addressed. To further tackle the unequal eye-openings in high-order-modulated systems, a higher number of signal paths for more accurate compensation is needed. For instance, an MRM-based PAM4 transmitter is reported in [3], where a highly parallelized driver architecture is designed. As depicted in Fig. 2(b), this driver consists of parallel driver slices digitally controlled by a reconfigurable array of lookup tables (LUTs). The LUTs are set to have the analog driver output counteracts the data-dependent MRM nonlinearities. That is, the parallel driver slices act as a segmented electrical digital-to-analog converter (DAC). With a sufficient number of slices/segments, the DAC can incorporate pre-emphasis and pre-distortion for overcoming the nonlinear modulation dynamics and intensity, respectively. The idea of segmentation can be alternatively carried out in the optical domain, thereby simplifying the electrical driver design. Shown in Fig. 2(c) is a two-segment MRM example [4]. By selectively driving the segment(s), the individual contribution to the change of the carrier density within the entire ring and thus the overall modulation of optical intensity at the output can be activated or deactivated. Along with encoders (e.g., LUTs) responsible for digitally setting the selection states, the segmented modulator functions as an optical DAC. The benefits of segmentation can also be accomplished by using multiple optical modulators; for example, two parallel electro-absorption modulators with uneven lengths are employed in [5]. To improve the DAC resolution for augmented adjustability of compensation, a higher level of segmentation is expected for both electrical DAC and optical DAC. In that case, the former would face challenges in the signal-path bandwidths due to the increased number of electrical connections, whereas the latter would result in overheads in the pin counts and area consumptions [3]. Besides, the optical-domain segmentation mostly fulfills the compensation for the nonlinear modulation intensity, but not for the nonlinear dynamics. At the expense of more driver slices, an electrical DAC can succeed in equalizing both types of nonlinearities by manipulating its driving force. In light of these trade-offs, co-design and co-optimization of electrical drivers along with optical modulators are crucial for effective and energy-efficient transmitter-side equalization.

IV. Conclusion

Transmitter-side equalization leverages the driver and/or modulator segmentation, combining the segment outputs in analog fashion to compensate nonlinearities, while digital nonlinear equalizers at the receiver-side serve as alternative or coexistent solutions robust to PVT variations. The proposed PWL equalizer, compared to its conventional Volterra equalizer counterpart, significantly improves the area and power efficiencies by avoiding explicit multiplicative computations for generating high-order terms.

References

[1] S. Lin, S. Moazeni, K. T. Settaluri and V. Stojanović, "Electronic–photonic co-optimization of high-speed silicon photonic transmitters," in Journal of Lightwave Technology, vol. 35, no. 21, pp. 4766-4780, 1 Nov.1, 2017, doi: 10.1109/JLT.2017.2757945.

[2] M. Raj, M. Monge and A. Emami, "A modelling and nonlinear equalization technique for a 20 Gb/s 0.77 pJ/b VCSEL transmitter in 32 nm SOI CMOS," in IEEE Journal of Solid-State Circuits, vol. 51, no. 8, pp. 1734-1743, Aug. 2016, doi: 10.1109/JSSC.2016.2553040.

[3] H. Li et al., "A 3-D-integrated silicon photonic microring-based 112-Gb/s PAM-4 transmitter with nonlinear equalization and thermal control," in IEEE Journal of Solid-State Circuits, vol. 56, no. 1, pp. 19-29, Jan. 2021, doi: 10.1109/JSSC.2020.3022851.

[4] A. Roshan-Zamir et al., "A two-segment optical DAC 40 Gb/s PAM4 silicon microring resonator modulator transmitter in 65nm CMOS," 2017 IEEE Optical Interconnects Conference (OI), Santa Fe, NM, USA, 2017, pp. 5-6, doi: 10.1109/OIC.2017.7965503.

[5] A. H. Talkhooncheh, A. Zilkie, G. Yu, R. Shafiiha, and A. Emami, "A 100 Gb/s PAM-4 silicon photonic transmitter with two binary-driven EAMs in MZI structure," accepted to 2021 IEEE Photonics Conference (IPC), 2021.