A 100 Gb/s PAM-4 Silicon Photonic Transmitter with Two Binary-Driven EAMs in MZI Structure

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***Abstract*—An integrated DAC-less PAM-4 transmitter in a multi-micron silicon photonics platform using 2 binary-driven uneven-length SiGe EAMs in an unbalanced MZI is presented. The optical transmitter exhibits 5.5dB ER at 100 Gb/s with 2.1dB SNR improvement compared to single EAMs driven by PAM-4 signals.**

Keywords—Silicon Photonics, PAM-4 Transmitter, Electro-absorption Modulator, EAM, Optical Interconnects, Unbalanced Coupler

I. Introduction

Highly-integrated optical interconnects in silicon photonics are growing as preeminent platforms for the next generation optical transceivers for inter- and intra-datacenter applications. Multi-level Pulse-Amplitude Modulation (PAM-N) is a promising modulation scheme that increases the overall bandwidth density efficiency. However, the inherent optical power penalty imposes demanding linearity requirements on analog link components, which results in power hungry electronics. The modulator type should be carefully chosen to satisfy transmitter specifications such as optical modulation amplitude (OMA), extinction ratio (ER), signal-to-noise ratio (SNR) and electro-optical power penalties. Travelling-wave and lumped phase modulators require relatively large voltages (large $V_\pi L$) and power-hungry electrical drivers while having lower bandwidth due to excessive microwave losses and large capacitive parasitics [1]. Despite their compact dimensions, silicon photonic ring modulators require careful temperature stabilization [2]. Electro-absorption modulators (EAMs) do not suffer from the mentioned limits due to their smaller footprints and lower voltage requirements, which make them attractive for high-speed modulation and dense integration with low pJ/bit energy efficiencies [3, 4, 5, 6]. However, their performance for PAM-4 is limited by transfer function linearity, input optical power and modulation chirp. In [7] a DSP-free 128 Gb/s PAM-4 silicon photonic transmitter using two binary-driven SiGe EAMs with even 120um length has been reported to eliminate above limits. The architecture, however, is not optimized for SNR and power penalty, and has device performance that is more sensitive to fabrication process variations due to the fixed input split ratio. Here we show an SNR-optimized design of a DAC-less 100 Gb/s PAM-4 transmitter using two binary-driven uneven-length SiGe EAMs placed in an unbalanced MZI structure, and experimentally demonstrate that this design improves the power penalty and SNR of the transmitter.

II. PAM-4 Transmitter Design

Generating equidistant PAM-4 power levels is achieved in various ways depending on the transmitter architecture. One method involves a non-equally-distanced PAM-4 electrical driver to modulate a single EAM. Alternatively, an optical PAM-4 is realized using 2 binary-driven EAMs. While placing 2 EAMs in series (segmented EAMs) would suffer from excessive insertion loss and limited optical input power, having them placed in parallel would break both limits, although, careful considerations for interferometric effects should be considered. The design variables of the MZI structure shown in Fig. 1(a), include the input optical power ($P_{in,a}$ and $P_{in,b}$), length of EAMs (L_1 and L_2), driver voltages (V_0 and V_1) and the coupling coefficient of the combiner (k_{out}). By setting target values for the outer OMA and the ER of the transmitter, the problem is reduced to a co-dependent system of 4 linear equations and 4 unknowns as shown in Fig. 1(b). This system has no real answers due to the resulting equidistant vector fields requirement, which are inconsistent with equidistant output power requirements (Fig. 1 (b)). As shown in Fig. 1(c), the field vectors (rather than the optical powers) from each arm are added linearly. One way to address this problem is to introduce a relative phase shift between the two arms such that the added field vectors generate equally spaced output power levels [6] This method, however, reduces power efficiency since a significant portion of power is lost as the relative phase shift between two arms increases. Another way is to use two intensity modulators (EAMs) with even-length and uneven input power split, such as 0.33:0.66 [7]. The output

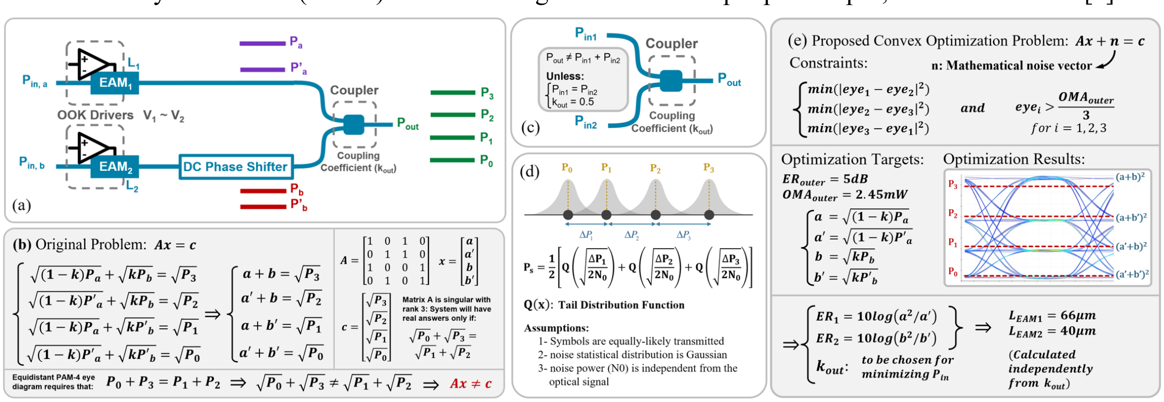

Fig. 1. (a) PAM-4 circuit optimization problem using EAMs in parallel, (b) Original PAM-4 problem, (c) Non-linear power addition at the optical coupler, (d) Symbol error rate for the unequally spaced PAM-4 transmitter, (e) proposed convex optimization problem for solving the unequally spaced PAM-4 Transmitter

OMA and the SNR could, however, be further optimized by using uneven lengths and unbalanced couplers. The proposed approach here is to solve for the 4 unknowns in presence of a mathematical noise vector, such that the overall SNR of the unequally-spaced PAM-4 levels (Fig. 1(d)) is maximized. This turns into a convex optimization problem shown in Fig. 1(e), for which, an outer ER of 5dB and an outer OMA of 2.45mW were chosen. In the resulting simulated eye diagram of Fig. 1(e), the optimized levels (in blue) are unequally spaced, however, the smallest eye (bottom) is still larger than the minimum eye closure requirement. Since simulation results are independent from k_{out}, it could be set independently to minimize the required input power. A sweep for k_{out} in Fig. 2(a) shows that the required input power is minimized at 0.39 (rather than 0.5). Such design optimization for SiGe FK-EAMs operating at 1550 nm wavelengths leads to the optimum EAM lengths of 66 µm and 40 µm.

III. Experimental Results

The photonic integrated circuit described in section II is fabricated in Rockley Photonics multi-micron Si-photonics platform, which is an EAM-based high-speed platform optimized for high density integration, low power consumption, and co-packaged optics [3, 4]. The unbalanced output combiner and the input power splitter are realized by MZI variable couplers using thermal phase shifters and multi-mode interference (MMI) devices (Fig. 2(b)). The targeted splitting and combining ratios are set by generating a relative DC phase shift for each variable coupler. Measurement setup is shown in Fig. 2(c). The optical signal is amplified prior to the chip to improve the SNR. Input power increase was only possible thanks to the parallel architecture, capable of receiving approximately double the amount of laser power without saturating the EAMs. Fig. 2(d) shows the 66µm EAM measured ER and IL spectra, while Fig. 2(e) displays the eye diagrams for a single EAM, as well as the proposed PAM-4 design, all driven at 50 Gbaud with 50Ω probes. The unbalanced MZI design exhibits 1.2dB better ER and 0.7dB better TDECQ at 50 Gb/s compared to a single EAM driven by an unequally-spaced and pre-emphasized PAM-4 driver. Moreover, at 100 Gb/s, the unbalanced MZI PAM-4 has 0.9dB better ER and 2.1dB better SNR. This scheme opens a pathway for sub-pJ/bit power consumption of EAM-based 100 Gb/s PAM-4 modulators, and a path to 200 Gb/s/λ by relaxing the combined requirements on EAM bandwidth, ER, and linearity for higher PAM-4 data rates. A DAC-based Bi-CMOS driver with a significant bias is required to drive a single EAM into its linear regime, but with this scheme two 2V CMOS NRZ 50 Gbaud drivers can be used [3], resulting in < 1 pJ/b of power consumption at 100 Gb/s.

IV. Conclusion

In this work, a silicon photonic PAM-4 transmitter with two uneven-length SiGe EAMs in parallel within an unbalanced MZI structure is demonstrated. The fabricated chip performs PAM-4 transmission at 100 Gb/s with 5.5dB ER and 2.4dB of TDECQ. This scheme can similarly be applied to design 100 Gb/s PAM-4 Si-photonic transmitters in the O-band using hybrid-integrated InP-based EAMs with < 1pJ/bit power consumption as well to provide a path to 200 Gb/s/λ transmitters.

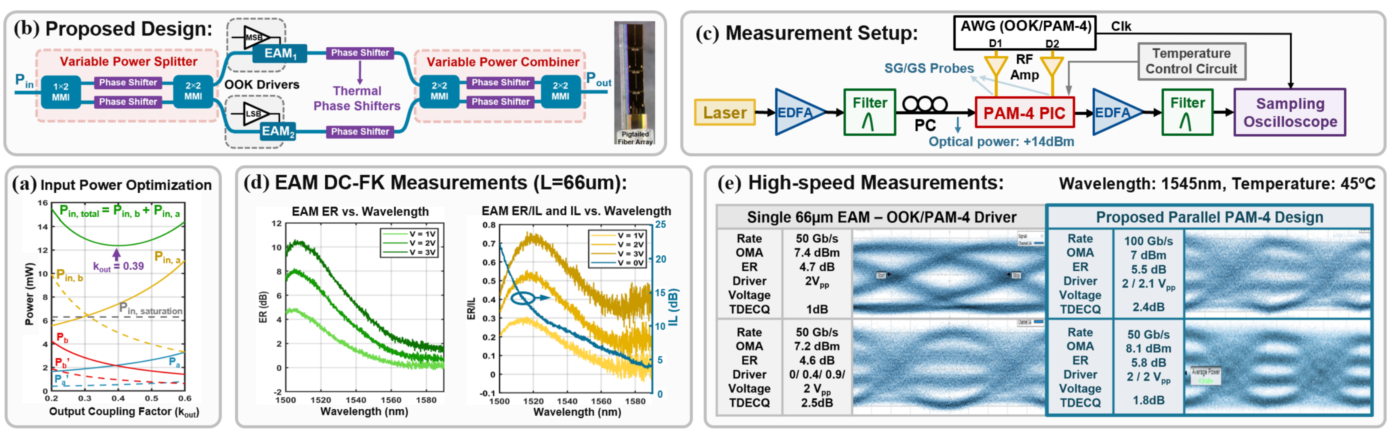

Figure 2. (a) EAMs' input power vs. combiner coupling coefficient, (b) Proposed PAM-4 transmitter chip layout, (c) Measurement setup, (d) Measured ER, IL and ER/IL spectra of a 66µm EAM under different bias voltages, (e) Eye diagrams for several configurations including the proposed PAM-4 chip

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