A Fully-Integrated Biofuel-Cell-Based Energy Harvester with 86% Peak Efficiency and 0.25V Minimum Input Voltage Using Source-Adaptive MPPT

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***Abstract*— This paper presents a cold-starting energy harvester in 65nm CMOS with source degradation tracking and automatic MPPT. A power-efficient architecture is proposed to keep the internal circuitry operating at 0.4V while regulating the output voltage at 1V using switched-capacitor DC-DC converters and a hysteresis controller. Peak efficiency of 86% is achieved at 0.39V input voltage and 1.34µW of output power with 220nW of internal average power consumption. Integrated operation with lactate biofuel cells is demonstrated.**

Keywords*— *Energy Harvester; Biofuel Cell; Source-adaptive MPPT, DC-DC voltage converter

I. Introduction

Recent advances in low-power electronics have paved the way for a wide range of wearable and implantable biomedical devices for health monitoring and fitness applications. Due to limited battery capacities at mm-scales, prototypes with wireless power delivery have been recently demonstrated [1, 2], but practical challenges limit their application. Alternatively, biofuel-cell (BFC) energy harvesting is gaining interest. BFCs with small surface area provide power at few-µW range and require energy harvesters that have high efficiency at such low power levels. Previous solutions often use bulky off-chip capacitors for energy storage because of the limited power and open-circuit (OC) voltage [3]. Energy harvesting systems developed for IoT applications suffer from loading condition dependencies [4], limited cold startup voltage requirements [5] and non-optimal power efficiency at few-µW loading conditions [6]. This paper presents a cold-starting energy harvester in 65nm CMOS with source degradation tracking and automatic MPPT to tackle these challenges. A combination of DC-DC voltage boost and buck converters with a hysteretic regulation approach is proposed to achieve 86% peak efficiency at 0.39V of input voltage and 1.34µW of output power. Moreover, energy harvesting and power delivery using an integrated BFC that utilizes lactate and oxygen as the fuel sources is demonstrated.

II. System Overview and Architecture

The top-level block-diagram of the energy harvester is shown in Fig. 1-a. It consists of a cold startup enhancement block which initially provides a direct path from the input voltage (V_{in}) to the low-voltage unit (shaded with gray). It powers up a low-voltage ring-oscillator, resulting in the whole chip's operation to start. A DC-DC switched-capacitor power converter (SCPC) then boosts the available input voltage by a reconfigurable conversion ratio (CR). The boosted voltage (VDDH) is regulated by a hysteretic controller between two programmable thresholds (V_{OH} and V_{OL} in Fig. 1-b, c, d), which could be set as per the load requirements. A dual-path DC-DC down converter converts VDDH to a lower level (VDDL = 0.4×VDDH) to supply all other critical sub-blocks. This reduces the internal power consumption significantly. Other blocks in the low voltage unit include an MPPT finite-state machine (FSM), 2 digitally controlled ring-oscillators (DCO) and a non-overlapping (NOL) clock generator. A low-power level-shifter is proposed to convert the voltage levels of clocking signals, which are delivered to the voltage converters. The proposed architecture ensures that the system performs a cold startup with a minimum input voltage of 0.39V and continues operation when it degrades to as low as 0.25V over time. In the following sub-sections, we discuss critical building blocks in more details:

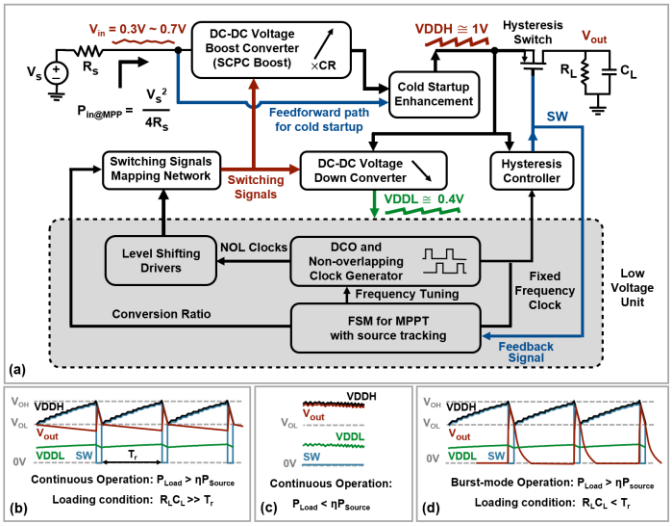

Fig. 1: (a) Top-level block diagram of the energy harvester; Various loading conditions depending on the application: (b, c) continuous (constantly delivering to a low-power sensor) and (d) burst-mode (for wakeup-enabled sensors with high power requirements).

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A. *Cold Start-up Enhancement Block:*

The cold startup enhancement block, shown in Fig. 2, consists of 4 low-V_{th} (LVT) PMOS switches to initially isolate VDDH from the output of the boost SCPC (V_{cp}) and the V_{cap} node with a 1.3nF storage capacitor (C_s). These switches are controlled by 2 latch-based comparators that dynamically compare VDDH to V_{cap} and V_{cap} to V_{cp}, respectively. At startup, signals S1 and S2, as shown in Fig. 2, are both zero so that the VDDH node is first pulled up to the input voltage (V_{in}). Therefore, the SCPC is bypassed and the internal blocks start operating. At the same time, C_s is being charged by V_{in} and V_{cp} is boosted by the SCPC. Once V_{cap} reaches V_{in} and V_{cp} reaches V_{cap}, S1 and S2 are switched to logic "high" by the comparators, respectively. This ensures a smooth supply transition from V_{in} to V_{cp} for the VDDH node as soon as the boost SCPC and C_s are ready.

B. *Dual-Path Down Converter Block:*

The first sub-block in the dual-path down converter is a low-dropout voltage regulator (LDO). As shown in Fig. 2, the LDO can be modeled as a controlled high-pass filter, in which the output (VDDL) initially follows the input voltage (VDDH) and then gets regulated at around 0.4V. This block is used at startup to deliver the initially available voltage to the internal circuitry to start the ring oscillator and the FSM. Once the cold start-up has taken place, the boost SCPC is clocked and VDDH reaches V_{OH}. The FSM detects this event and switches the down-conversion path from the LDO to the more power-efficient buck SCPC by the S3 signal. The switched-capacitor buck converter continuously multiples VDDH by 2/5 through cascading a standard ×1/5 voltage divider with a voltage doubler.

C. *Switched-Capacitor DC-DC Boost Converter (SCPC):*

The boost SCPC consists of 4 stages of interleaved voltage doublers, each performing a ×1, +1 or ×2 operation. Fig. 3-a shows the details of each stage. PMOS and NMOS transistors are used for both the high-side and the low-side switches for a minimal ON resistance, especially when the switching signals have lower swings at startup. PMOS switches are avoided for ground connection of bottom plates of the flying capacitors since they provide a shorted path from V_{in} to the ground at startup. Each transistor is sized individually for an optimum ON resistance, gate capacitance, and isolation (when turned off).
For an efficient performance, voltage levels of the clocking signals applied to the gates of the switches should always be shifted from VDDL to VDDH. An optimization analysis is performed to find out the placement order of the level shifters and the mapping network. Considering the total number of SCPC switches (54 for boost + 88 for buck) and the average activity factor of all mapping network circuitry (which depends on the chosen CR), placing the level shifters first, saves power by 40% (Fig. 3-b).

D. *Low-Voltage Digitally Controlled Ring Oscillator (DCO):*

The digitally controlled ring oscillator operates at a minimum of 0.25V supply and provides clocking signals to the voltage converters through the NOL clock generator. It consists of two thyristor-based delay cells and a buffer (Fig. 3-b). In each delay cell, transistors M1 and M4 first reset the block by having a pulse signal at their gates. Subsequently, the drain voltages of M2 and M3 start accumulating/dissipating charge through the leakage current paths that M1 and M2 provide. The outputs then switch through the positive feedback loop that is formed by M2 and M3. The duration of this transition (hence, the frequency of the oscillator) is adjusted by the binary-weighted branches of sub-threshold transistors. Minimum-size LVT transistors are chosen for M1 and M4 to minimizes the overall power consumption while providing enough leakage current. M2 and M3 mainly operate in sub-threshold and are chosen to be HVT to be more robust across process corners.

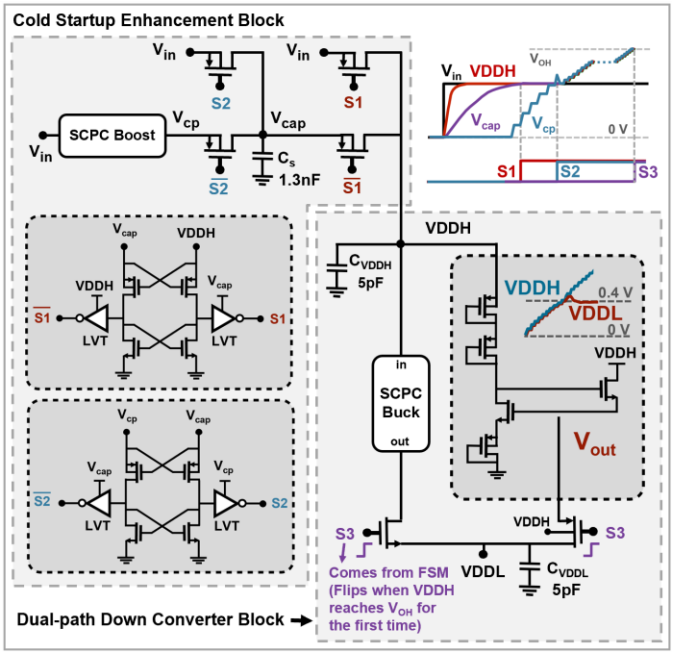

Fig. 2. Cold startup enhancement and the dual-path down converter blocks.

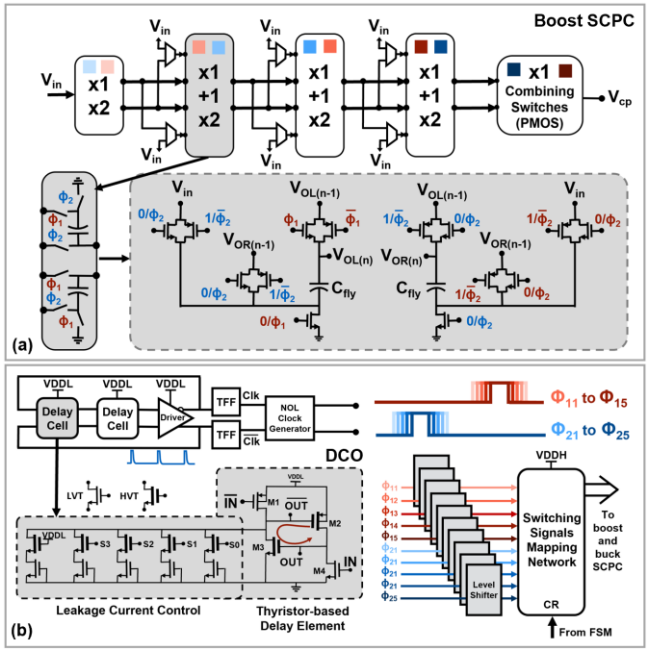

Fig. 3. (a) Boost SCPC with non-overlapping switching signals
(b) DCO (left) and SCPC switching signals mapping architecture (right).

E. *Level Shifters:*

The level shifters are used to change the voltage levels of several logic and clock signals from VDDL to VDDH, while maintaining the timing margins of the non-overlapping clocks. The proposed level shifter circuit is shown in Fig. 4. At startup, when both VDDH and VDDL are below V_{in}, the input signal is passed through the LVT inverter path followed by the LVT buffer, since no level shifting is required, and transitions should be made as sharp as possible. When the voltage levels increase, the level shifter path along with the HVT buffer is activated to avoid burning excessive power in the LVT inverters due to dynamic short currents. The level shifter sub-block consists of a stacked and cross-coupled structure to enhance the gain. This architecture ensures that the level-shifting operation is feasible under all combinations of VDDL and VDDH from 0.4V to 1V. An identical level shifter with a fixed input of VDDL is used to generate the LS signal for all other level shifter blocks. A high output implies that the level shifters are ready to detect a signal with the current VDDL amplitude.

F. *Hysteresis Controller and MPPT with Source Tracking:*

The hysteresis controller block (Fig. 4) consists of two clocked comparators that compare VDDH to V_{OH} and V_{OL}. This comparison is performed by using a programmable voltage divider ladder for VDDH and a bandgap reference. Depending on the loading conditions, VDDH is either kept between V_{OH} and V_{OL} or gets saturated (above V_{OL}) using a hysteresis switch that connects the VDDH node to the load (V_{out}).

The MPPT controller is an FSM synthesized with HVT transistors supplied by VDDL to reduce the dynamic and leakage power consumption. As shown in Fig. 5, It initially generates a default CR for the boost SCPC to charge VDDH towards V_{OH}. Once VDDH approaches V_{OH} for the first time, the FSM switches the down converter path from the LDO to the buck SCPC. The 2D MPPT is then performed by minimizing the time that it takes (T_r) for VDDH to rise from V_{OL} to V_{OH} with a linear search for the optimum CR value (coarse tuning) followed by the switching frequency (fine tuning). This scheme makes the whole process independent of the loading conditions. If a change in the locked T_r is detected, the circuit will redo the MPPT, starting from the latest locked CR (source tracking).

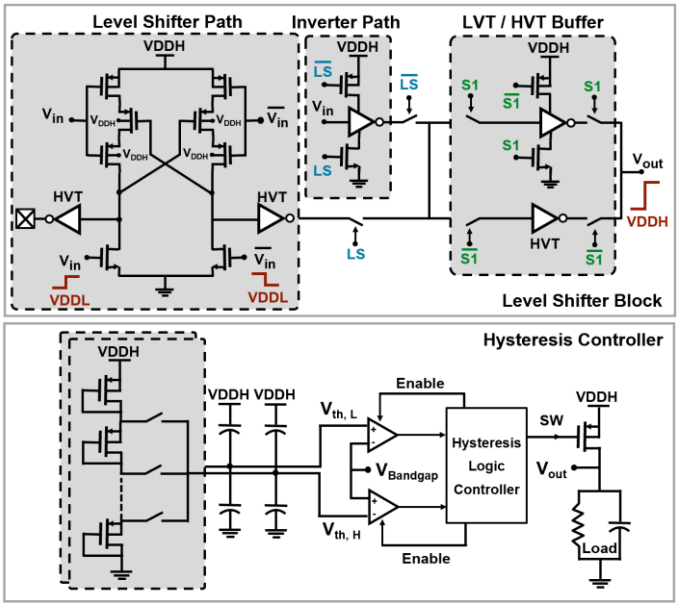

Fig. 4. Dual-path level shifter block and Hysteresis controller circuit details.

III. Measurement Results

The energy harvester chip is fabricated in a 65nm CMOS process. The circuit performs cold startup and automatic MPPT with an input OC voltage of at least 0.39V and an average input power (P_{in}, defined as the maximum deliverable power) of 1.56µW, as shown in Fig. 6-a. Peak power efficiency of 86% is achieved with 220nW of internal power consumption.

Three more experiments are shown in Fig. 6. In one case (Fig. 6-b), the input voltage is first decreased from 0.6V to 0.5V to mimic a degradation in the BFC energy source while delivering power to an internal 60 kΩ test resistor. As shown in Fig. 6-b, the system first detects a change in the rise-time of VDDH. Then the CR value and the switching frequency are modified to find the new MPP. The loading condition for this case is set to mimic high-power burst-mode operated sensors. In another case (Fig. 6-c), the output power is comparable to the loading condition (1 MΩ external resistor). The input OC voltage is decreased to 0.25V after MPPT lock and the average input power is set to 2.25µW, while V_{out} settles to 1.01V. In the last case (Fig. 6-d), a continuous mode operation for a capacitive loading condition is demonstrated, in which the instantaneous P_{Load} is more than P_{out}. VDDH is still regulated while V_{out} remains above 0.9V.

In an in-vitro experiment, a pair of biofuel-cells with a 2mm diameter is used to extract energy in a 20 mM lactate solution (Fig. 7). The OC voltage is initially 0.56V with approximately 5.9µW of average input power. The circuit performs cold startup and locks at the MPP with 3.1µW of average power delivered to an internal 60 kΩ test resistor. The OC voltage degrades to 0.39V after 10 minutes and then to 0.25V after 30 minutes, while the chip continues its operation. The die micrograph and the PCB are shown in Fig. 8. A power efficiency analysis in Fig. 9 and comparison with prior art in Table 1 shows the overall performance of the energy harvester.

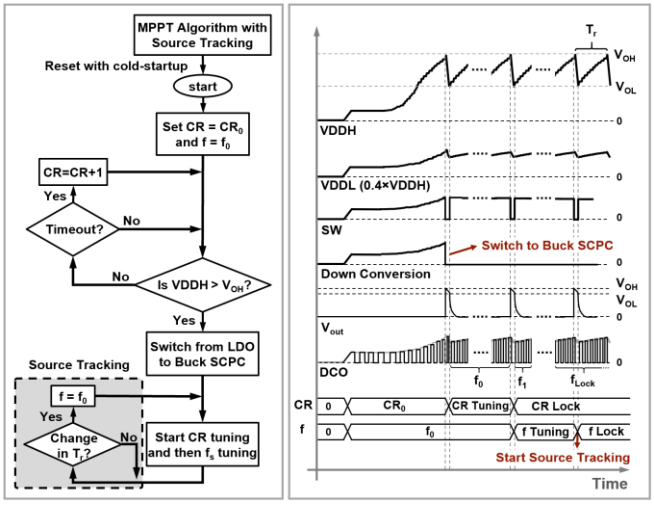

Fig. 5. Flow chart and timing diagrams of the proposed MPPT algorithm.

Benefiting from the proposed architecture, a superior efficiency with less than 0.4V of input voltage and 5.5µW of average output power is achieved by the energy harvester.

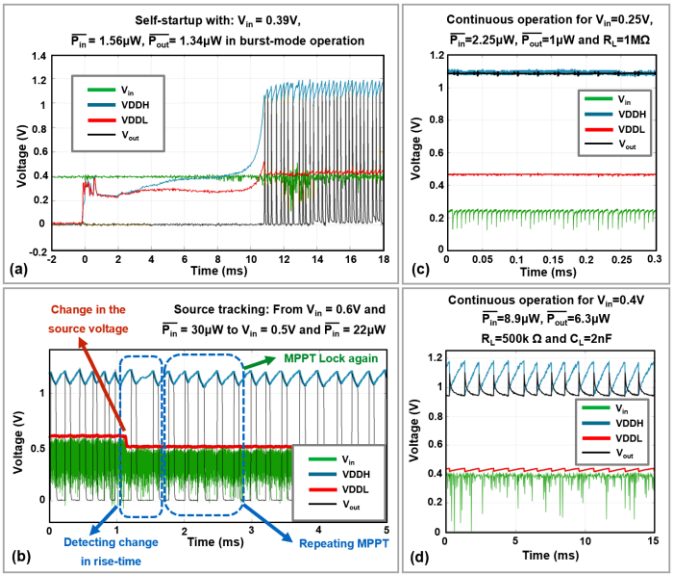

Fig. 6. Measurement results:
(a) cold startup in burst-mode sensing (b) source-adaptive MPPT;
Continuous supply for V_{out} (c) when $P_{Load} > P_{out}$ and (d) when $P_{Load} < P_{out}$.

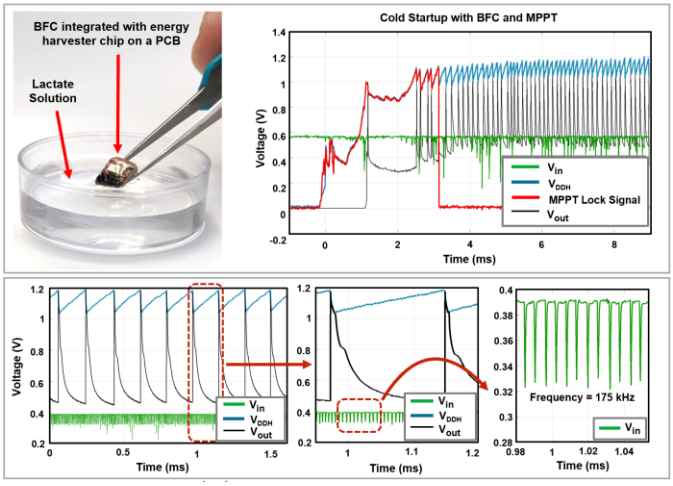

Fig. 7. In-vitro measurement test setup with lactate BFC, demonstrating cold start-up and MPPT (top right) and tracking the source OC voltage degradation from 0.56V to 0.39V over time (bottom).

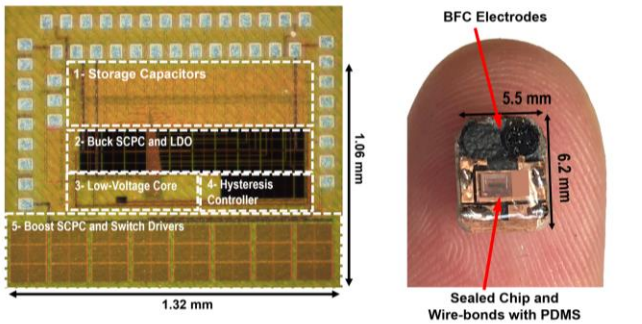

Fig. 8. 65nm CMOS Chip Micrograph and the PCB with BFC and the chip.

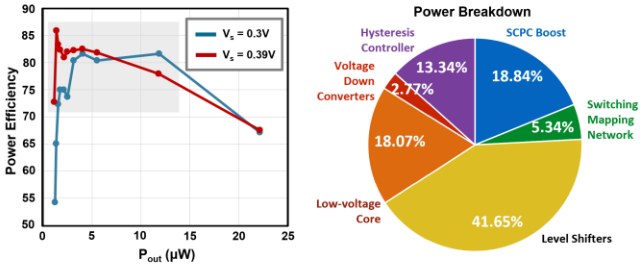

Fig. 9. Measured efficiency plots of the energy harvester and simulated power breakdown of the internal circuitry.

TABLE I. COMPARISON WITH PRIOR ART

	[3] JSSC'18	[4] JSSC'16	[5] JSSC'18	[6] TCAS-I'18	This Work
Technology	65 nm	0.18 um	65 nm	0.18 um	65 nm
Fully Integrated	No	Yes	Yes	Yes	Yes
Source Type	BFC	TEG / PV	TEG / PV	PV	BFC
Topology	Duty-cycled	Boost SCPC	Boost SCPC	Boost SCPC	**Boost + Buck SCPC**
MPPT	Matched resistor	2D	3D	2D	2D
Output Voltage (V)	0.3	3.3	1	1.2 - 1.8	0.9 – 1.5
Input Range (V)	0.3 - 0.5	0.45 - 3	0.35 - 1	0.5 - 1.8	**0.25 - 1**
Min Cold Startup (V)	0.3	2.1	0.35	0.72	0.39
Frequency Range	100 Hz	27 kHz – 1 MHz	19 kHz – 16 MHz	25 kHz – 1 MHz	100 kHz – 2 MHz
Output Power (µW)	400 – 800	< 50	0.1 – 300	5.9 – 35.1	1 – 100
Peak Efficiency	N/A	81% @ 1.2V and 16µW	88% @ 0.85V and 200µA	72% @ 1.2V and 35µW	**86% @ 0.39V and 1.34µW**
Efficiency at BFC-level source power		42% @ 0.6V and 1µW	70% @ 0.5V and 5µA	66% @ 0.9V and 6µW	**80.1% @ 0.3V and 5.5µW**
Chip Active area (mm²)	0.58 [a]	2.89 [a]	0.54	0.55	1.4

[a] Estimated from provided figures

REFERENCES

[1] A. Agarwal et al., "A 4µW, ADPLL-based implantable amperometric biosensor in 65nm CMOS," 2017 Symposium on VLSI Circuits, Kyoto, 2017, pp. C108-C109.

[2] H. Lyu, et al., "A 430-MHz Wirelessly Powered Implantable Pulse Generator With Intensity/Rate Control and Sub-1 µA Quiescent Current Consumption," IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 1, pp. 180-190, Feb. 2019

[3] A. F. Yeknami et al., "A 0.3-V CMOS Biofuel-Cell-Powered Wireless Glucose/Lactate Biosensing System," in IEEE Journal of Solid-State Circuits, vol. 53, no. 11, pp. 3126-3139, Nov. 2018.

[4] X. Liu et al., "A Highly Efficient Reconfigurable Charge Pump Energy Harvester With Wide Harvesting Range and Two-Dimensional MPPT for Internet of Things," in IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1302-1312, May 2016.

[5] K. Rawy, T. Yoo and T. T. Kim, "An 88% Efficiency 0.1–300–µW Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes," in IEEE Journal of Solid-State Circuits, vol. 53, no. 10, pp. 2751-2762, Oct. 2018.

[6] X. Liu, K. Ravichandran and E. Sánchez-Sinencio, "A Switched Capacitor Energy Harvester Based on a Single-Cycle Criterion for MPPT to Eliminate Storage Capacitor," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 2, pp. 793-803, Feb. 2018.