# Optical Interconnects: Design and Analysis

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**Abstract:** This paper focuses on design challenges and solutions for realization of low-power high-speed electronics for optical interconnects. Design methodologies for high sensitivity receivers and optimized driver circuitries at the transmitter side are presented.
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## 1. Introduction

Optical signaling is considered a key technology in realization of the next-generation networks and interconnects. The main advantages of optics stem from providing an ultra-high frequency carrier, allowing large bandwidth densities and transmission over longer distances. It is projected that mega-datacenters and high-performance computers (HPC) will continue to scale and deploy optical interconnects to meet the required aggregate bandwidth. It is also expected to achieve high levels of integration with low manufacturing costs using integrated silicon photonics (SiP) infrastructure and wavelength-division-multiplexing (WDM) technology. In addition to bandwidth density and low cost, for optical interconnects to become viable and dominate, their total power consumption needs to fall below electrical links. The required electronics and integrated circuits at the interface of communication and computation not only set the electronic domain power of the link, but also impact the power in the optical domain. This is because the laser output power is a strong function of sensitivity of the receiver and modulation quality at the transmitter, both greatly affected by the electronics as well as photonic devices with trade-offs entangled between the two domains. Therefore, a holistic approach is essential to achieve the optimum energy efficiency at the target bandwidth density with co-design of electronics and photonics, leading to co-optimization of transmitter, receiver and clocking modules. In this paper, we discuss the main challenges for the electronics at the receiver and transmitter sides. We also present examples of enabling approaches toward high bandwidth density and low power consumption in optical interconnects.

## 2. High-speed, high-sensitivity receiver design

Receiver front-end is one of the most important building blocks of any optical interconnect. It greatly impacts the overall energy-efficiency (energy-per-bit in fJ/bit) of the link, not only at the receiver side, but also by defining the required laser power and OMA of the transmitter. Depending on the photonic device performance and losses in optical couplings, the overall link power is set by the trade-offs between receiver's sensitivity and power.

The simplest optical receiver front-end can comprise of a passive resistor, which converts the current of the photo-detector (PD) $I_{op}$ to a voltage swing $\Delta V = RI_{op}$ in Fig. 1a, followed by gain stages. However, the direct trade-off between bandwidth (BW) and signal-to-noise ratio (SNR) in such design is often prohibitive (unless equalization techniques are employed). This is because $BW \propto (RC)^{-1}$ (limited by the pole at the input node) and $SNR \propto RI_{op}$. For a target SNR, which sets the bit-error-rate (BER) of the link, small $R$ translates to large $I_{op}$ requirements and degraded sensitivity. The effective input resistance of the front-end can be reduced significantly by adding an active gain stage to create a transimpedance architecture (TIA), which allows higher gain for a given input pole frequency, Fig. 1b. The addition of the active stage, with transistors and other components, increases the noise and power consumption. Nevertheless, with a careful design, at a given BW, higher SNR is achievable.

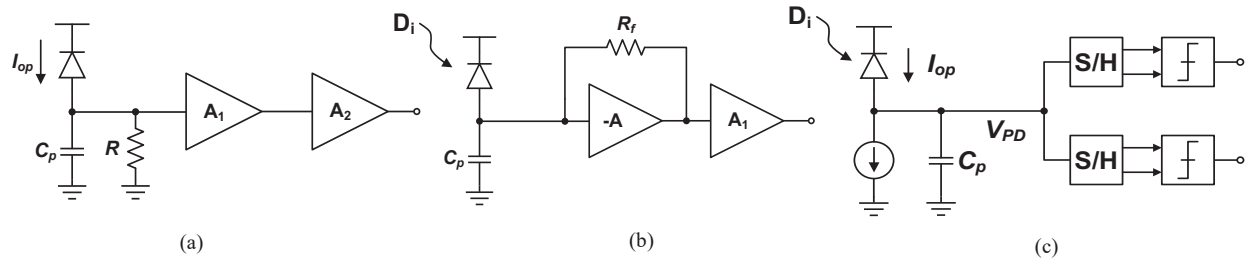


Fig. 1 Optical receiver front-end topologies; (a) passive resistor, (b) TIA, (c) integrating

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As the data-rates scales to beyond 25Gbps per channel, the bandwidth and noise requirements of the main amplifier and following stages in Fig. 1b become more and more difficult to meet in standard CMOS processes. If the gain of these amplifiers decreases at high frequencies, all the advantages associated with the TIA diminish. While using scaled CMOS technologies can provide more bandwidth, the reduction of voltage headroom and output resistance of transistors introduce new challenges and limit the choices of topologies for these analog circuits. On the other hand, recent development of photo-detectors with extremely low capacitances combined with advanced integration techniques (3D or monolithic) that add very low or negligible parasitics [3], create opportunities to develop new high-performance CMOS front-end architectures.

In order to avoid high bandwidth analog amplifiers in highly scaled CMOS technologies, it is very attractive to replace such building blocks with "mostly-digital" components, where transistors behave as switches. A possible architecture toward this goal, described in [1], creates an integrating node at the input and removes the resistive current-voltage conversion approach of TIAs. The current of photo-detector $I_{op}$ is integrated onto the capacitor at the input ($C_P$+$C_{in}$), and two sample-and-hold (S/H) switches are employed to sample the voltage signal at the input ($V_{PD}$). The subsequent stage is a clocked comparator, which effectively realizes a "differentiator" by comparing two consecutive samples of the input waveform, Fig. 1c. Therefore, the output of the comparator represents the original data signal. This architecture can support very high data rates with small power consumption by removing the TIA feedback loop and high bandwidth analog amplifiers. In order to achieve high sensitivity, precise calibration of comparators (sense-amplifiers in [1]) for offset removal is essential. Major challenges with the integrating front-ends are headroom (voltage swing) control and sensitivity degradation due to charge sharing and noise associated to S/H, as direct consequence of removing the analog amplifier and feedback. These challenges become more important as both CMOS and SiP technologies advance; voltage headroom and PD/bonding capacitances are reduced. From frequency domain perspective, the high-speed TIA creates a very high-frequency pole at the input node, which is comparable to the bandwidth of input signal (half of data rate). The integrating front-end on the other hand, creates a "zero frequency" pole at the input. An alternative middle-ground solution is to create a non-zero pole at the input with a frequency that is still much lower than the data rate, BW<<1/$T_b$, where $T_b$ is the bit period, Fig 2. This condition can be created by either adding a relatively large resistor at the input node [2] or by using a low-bandwidth (LBW) TIA [3]. In both cases the front-end operates very similar to an integrating front-end, but the added resistor or LBW-TIA will help with the headroom control. The same circuitry as integrating front-end (S/H plus comparator) can be used to recover the data if the offset of comparator is modulated based on the voltage level of the input to compensate the low-frequency pole (called dynamic offset modulation or DOM in [2,3]). The LBW-TIA has the additional benefit of providing isolation between sampling capacitors and PD capacitor to enhance the sensitivity. This is particularly attractive when the PD/bonding capacitors fall below 100fF. The proposed architecture was implemented in ST 28nm CMOS, 3D integrated with the SiP chip by CEA-Leti. It achieves -14.9dBm of sensitivity and energy efficiency of 170fJ/b at 25Gb/s with BER<$10^{-12}$. A similar topology in a 4-channel WDM architecture supports 32Gbps of data rate with 150fJ/bit of energy efficiency in ST 28nm FDSOI technology.

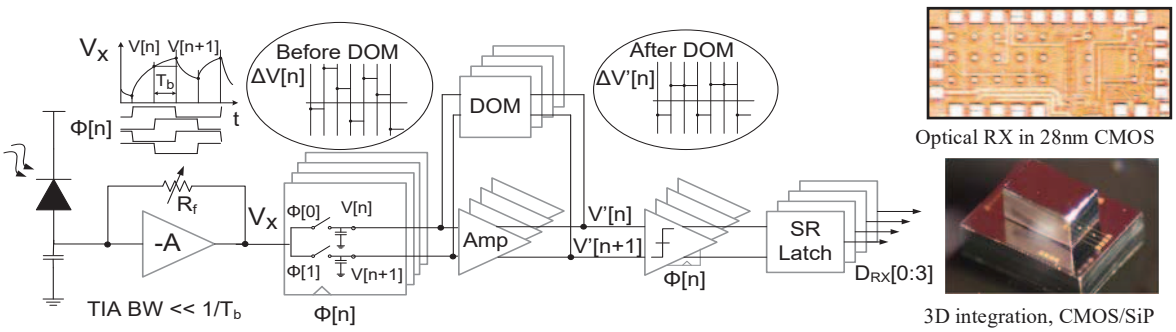


Fig. 2 Integrating front-end with LBW TIA and dynamic offset modulation, 3D integrated with SiP photodetector and grating coupler [3]

## 3. High-speed optical transmitter design

At the transmitter side, direct and external modulations have both demonstrated promising performances in recent years. The design of electronics that drive the laser or modulator is greatly affected by the characteristics of the optical device and the required output OMA, which is set by the link losses and receiver sensitivity. The overall power consumption at the transmitter side, which includes the power of electronics and the laser source can be a

significant portion of overall power consumption of the link. At very high data rates and assuming that the receiver is optimized for best sensitivity, the switching power of electronics can become comparable or even greater than the laser power consumption. Enhancing the sensitivity of receiver can reduce the switching power of transmitter electronics as well as the laser power by relieving the OMA requirement, and therefore voltage (or current) swing requirements of driver circuitries. Transmitter design thus requires careful optimization and co-design of electronics and photonics with an eye on the receiver trade-offs. In particular, accurate modeling of the optical devices in electrical domain, or with equivalent electrical components, is extremely important. The models should include not only the main function and parasitic components, but also non-linearity, noise sources and optical dynamics. Such modeling will enable electronic designers to take advantage of electrical domain techniques such as pre-emphasis and non-linear equalizations to enhance the performance of the transmitter. In [4] by accurately modeling/representing the non-linearity and optical dynamics of the VCSEL in electrical domain, a non-linear optimized pre-emphasis technique is proposed and implemented. By having different equalization taps for rising and falling edges, and optimizing the pulse width $t_{eq}$, the VCSEL operates at high data rate with very low bias current, pushing the device performance beyond its nominal bandwidth, Fig. 3. It also led to the important observation that $t_{eq}$ is only the function of bias current of the laser, which allows adaptive adjustment of $t_{eq}$ as the bias current changes. The VCSEL driver in 32nm SOI CMOS consumes less than 0.77pJ/bit while enhancing the data rate of the VCSEL to 20Gbps [4] using the proposed non-linear equalization approach.

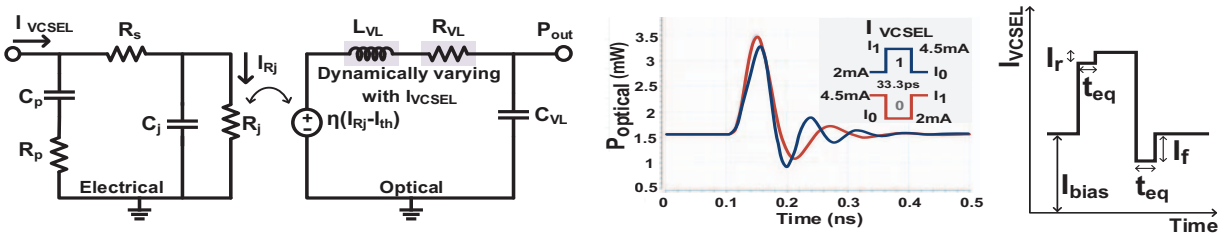


Fig. 3 Non-linear model of the VCSEL, overlaid pulse responses of VCSEL for isolated "0" and "1" bits, and equalized drive waveform [4]

External modulators provide an opportunity to achieve very high modulation rates while employing efficient high-quality sources especially for dense WDM architectures. The power efficiency and speed of driver circuitry are greatly affected by the modulator requirements and characteristics. Micro-ring modulators (MRM) have gained a lot of attention over the past decade due to their compact size and low power consumption, but they require tuning and thermal control. Examples of such structures include carrier-depletion and carrier-injection micro-ring modulators in the SiP platform. Carrier depletion MRMs have higher bandwidth compared to the injection mode MRMs, but require higher voltage swing for an acceptable extinction ratio. This voltage can be well above CMOS-compatible voltage headroom of around 1V. Stacked topologies and pulsed-mode pre-drivers have been proposed to deliver high voltages without stressing the transistors in the final stage of the push-pull [5]. Carrier-injection MRMs on the other hand require relatively small voltage swings, but they have limited bandwidth due to their slow carrier dynamics. In [6] an ultra-low-power pre-emphasis approach is demonstrated to achieve significant BW enhancement for injection-mode MRM. In this design, a monolithic temperature sensor enables an integrated thermal control loop.

## 4. Conclusion

Future energy-efficient and high-BW optical interconnects require a holistic approach via co-design of electronics and photonics, as well as co-design of receiver and transmitter components. Overall link optimization considering trade-offs between receiver sensitivity, receiver power, driver power, voltage swing, and laser power is essential.

## 5. References

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