A 16-Channel 1.1mm^2 Implantable Seizure Control SoC with Sub-µW/Channel Consumption and Closed-Loop Stimulation in 0.18µm CMOS

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Abstract

We present a 16-channel seizure detection system-on-chip (SoC) with 0.92µW/channel power dissipation in a total area of 1.1mm² including a closed-loop neural stimulator. A set of four features are extracted from the spatially filtered neural data to achieve a high detection accuracy at minimal hardware cost. The performance is demonstrated by early detection and termination of kainic acid-induced seizures in freely moving rats and by offline evaluation on human intracranial EEG (iEEG) data. Our design improves upon previous works by over 40× reduction in power-area product per channel. This improvement is a key step towards integration of larger arrays with higher spatiotemporal resolution to further boost the detection accuracy.

Introduction

Patients with intractable epilepsy can benefit from devices that perform automatic seizure detection and responsive stimulation [1-3]. Available EEG-based systems (e.g.[1]) are non-invasive, but suffer from limited resolution and high susceptibility to artifacts. Utilizing intracranial EEG signals [2, 3] improves the seizure detection accuracy, but inevitably poses tight power and area constraints on the implantable system. Integrating a large number of wide-BW iEEG channels discourages the application of conventional methods, such as spectral energy extraction in multiple bands or frequency spectrum computation. Specifically, extracting features from each channel separately requires either a dedicated ADC or extra TDMs and buffers. It also increases the dimensionality of feature space, potentially degrading the classification performance due to the curse of dimensionality.

In order to efficiently exploit multi-channel data in dense iEEG arrays, we combine every 16-channel x_i into a single $\tilde{x}$ using a linear spatial filter with i.i.d. random Bernoulli weights (w) [4]. The combined signal $\tilde{x}$ (Fig. 1) not only contains the essential discriminative information for epileptic activity classification, but also the crucial information for offline reconstruction of the original channel signals based on Compressive Sensing theory. Compared to [4] which relied on a single feature to detect seizures, this work integrates an optimal set of features and additionally includes a responsive closed-loop neural stimulator, with the full system verified in-vivo. This design improves the state-of-the-art by over 40× reduction in power-area product per channel and is readily scalable to larger arrays, given its small area and low power.

System Architecture

The proposed system architecture is shown in Fig. 1. Each front-end channel incorporates a dual-stage capacitive-coupled (CC) fully differential low-noise amplifier. The analog outputs of the amplifiers pass through a low-power (320nW) SC spatial filter followed by an 8b SAR ADC employing an area-efficient binary-weighted split array (total capacitance: 3.3pF). The feature extraction processor is subsequently activated. Upon seizure detection, the current-mode neural stimulator is triggered to suppress impending seizures.

Fig. 2 shows the AFE and spatial filtering stage (SFS). The first-stage CC-LNA provides a gain of 30dB at a small input capacitance (1.5pF) and bias current (700nA). A conventional CC topology with reduced-size unit capacitors is employed in the second stage (12dB). The SFS is composed of a SC summing amplifier that performs the $w^T x$ vector multiplication. The feedback attenuation factor (C_F/C_i) is adjustable by switching in the required number of unit capacitors. Through channel multiplication by 0 or 1, the dynamic range is efficiently boosted to accommodate the full-scale ADC input. Fully-differential folded-cascode OTAs are implemented in channels, while a two-stage OTA with rail-to-rail swing is utilized in SFS.

The seizure detector unit extracts four time-domain features mathematically defined in Fig. 3. In addition to widely used power and line-length features [5], the correlation of maxima and minima in successive iEEG windows is used to capture the high-frequency oscillations (HFOs). Lastly, the moving average of absolute value is computed, as a fast and sensitive but moderately specific detector. In a patient-specific training phase, the single optimal feature, or a logical combination of features is assigned to trigger the stimulator. To reduce detection delay, feature vectors are calculated for windows of length 256 (64ms at 4kS/s). The detection flag is raised upon 3 consecutive threshold crossings to limit the number of false positives. The data collector provides parallel threshold input to the arbiter, while the raw feature vector is generated at the output of a 16b PISO. Combined with stimulator logic, FE consumes 240nW at 4kHz CLK and 0.8V supply, 68% of which is leakage.

Fig. 4 shows the architecture and timing diagram of the stimulation block. Upon seizure detection from a 16-channel subset of electrodes, an adjustable charge sequence is delivered to the stimulation site. Biphasic pulses with 5b varying amplitude (<818µA), frequency (<1kHz), width, and burst duration (BD) are generated at the output of the current driver with a gain of 8, avoiding extra power consumption in the bias branch of binary DAC. In non-seizure mode, the entire current of stimulator including the static bias of DAC and output driver is turned off.

Experimental Results

The individual front-end channel draws 1µA from a 0.8V supply, has a midband gain of 42dB (Fig. 2), and exhibits an integrated input-referred noise of 5.9µV$_{rms}$ (10Hz-10kHz) and NEF of 2.94. Fig. 2 further presents the measured time-domain output of SFS for sample iEEG signals applied to the chip.

The measured output voltage of stimulator using a 1kΩ resistive load is shown in Fig. 4, with a measured current mismatch of 0.7% at 560µA. The stimulator consumes 360µW from a 3.3V supply (560µA, 200Hz) at continuous stimulation mode. Since the entire SoC operates in a closed loop, the stimulator is rarely active and has a negligible contribution to total power of the system.

Fig. 5 shows the results of an in-vivo study of the proposed system in a freely moving adult Wistar rat, implanted with 16 recording electrodes in neocortex and hippocampus and a pair of

stimulating electrodes in hippocampal commissure. Epileptiform activities were evoked by injection of 0.4µg/0.2µl kainic acid into left dorsal hippocampus. Using the logical conjunction of four criteria, the seizure events are successfully detected and suppressed by responsive stimulation, as shown in Fig. 5. During a four-hour continuous iEEG monitoring, 93% of total seizures (25 of 27) were successfully detected with a maximum delay of 0.5s, and subsequently terminated by responsive stimulation (reviewed by an epileptologist).

Our seizure detection algorithm was further evaluated offline, using 420h of human iEEG data containing 23 seizures from four patients at Bern University Hospital. It achieved a sensitivity of 100% and an average false alarm rate (FAR) of 0.15/h, improving the specificity by 56% compared to [4].

Fig. 5 presents the chip micrograph and layout of a front-end channel implemented in 0.18µm CMOS. This system improves the state-of-the-art in terms of both power consumption and chip area while maintaining a reasonable accuracy, as shown in the comparison table.

References

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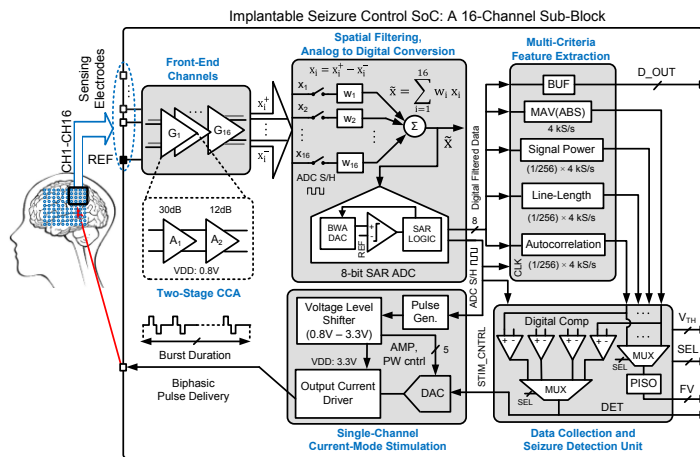[5] L. Logesparan et al., *Med Biol Eng Comput*, 2012.

Fig. 1 Architecture of the proposed closed-loop seizure control system.
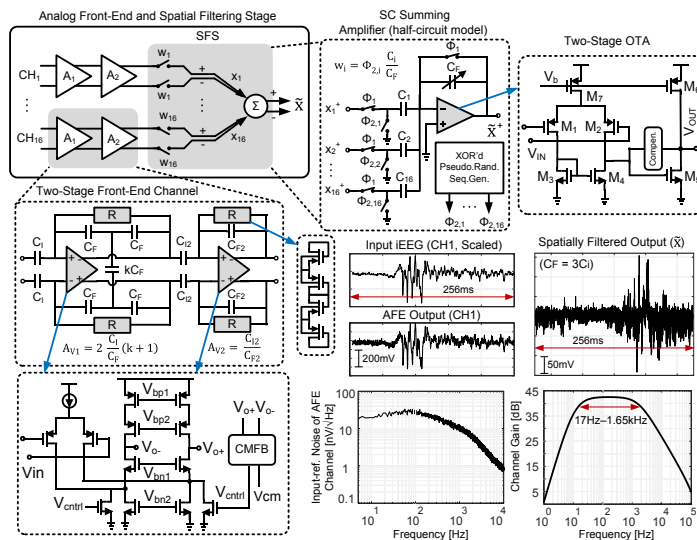

Fig. 2 AFE and SFS circuit diagrams with measured time-domain outputs, input-referred noise and gain of channels.
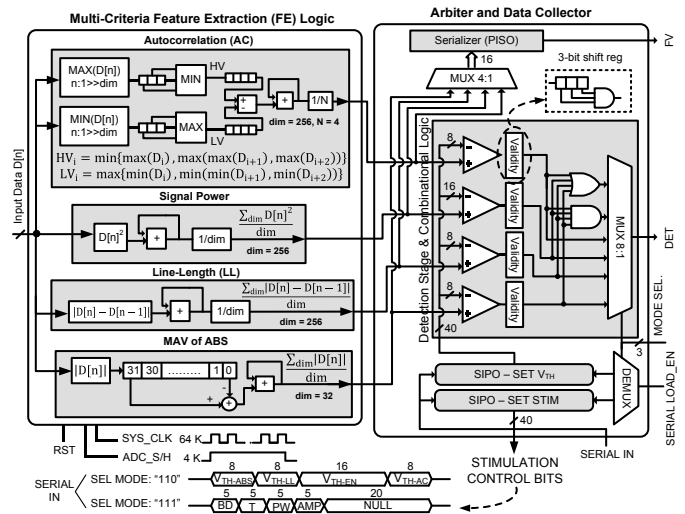

Fig. 3 Seizure detection processor including the feature extraction blocks, arbiter, and the data collector.
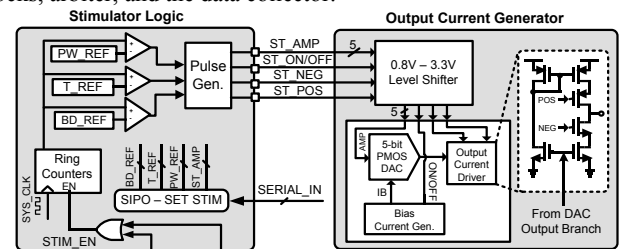

Fig. 4 Current-mode neural stimulator, the corresponding timing diagram, and measured output voltage on 1kΩ resistive load.
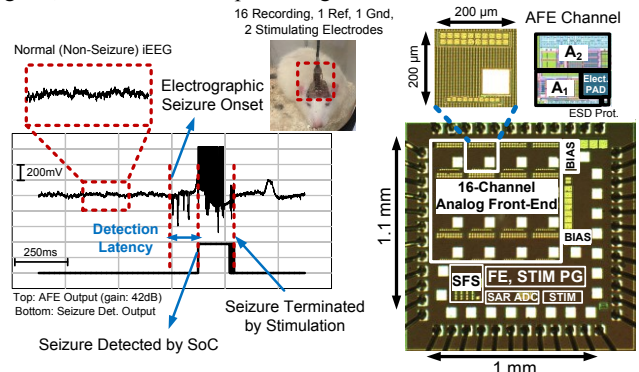

Fig. 5 (Left) In-vivo test results of the closed-loop SoC. (Right) Die micrograph and layout of front-end channels.

Table 1. Performance Summary and Comparison

Parameter	[1]	[4]	[2]	[3]	This work
Technology (CMOS)	0.18µm	0.18µm	0.18µm	0.13µm	0.18µm
Signal Modality	EEG	iEEG	iEEG	iEEG	iEEG
Chan. Count	1 to 16	16	8	64	16
Area [mm²]	25	1[d]	13.46[a]	12[b]	1.1[d]
Closed-Loop	YES	NO	YES	YES	YES
Feature Type	FTDM-BPF	LL	Entropy, Freq. Spect.	Mag, Phase, PLV	Energy, LL, AC, ABS
Multi-Feature Detection	NO	NO	YES	YES	YES
Bandwidth [Hz]	0.5–100	30–1.7k	1–7k	1–5k	17–1.65k
Sample Rate/Chan.	1kS/s	4kS/s	62.5kS/s	54kS/s	4kS/s
Power	-	13.6µW	2.798[a]mW	1.4[c]mW	14.8µW
Sensitivity (%)	95.7	100	92	100, 70	100
FAR (Specificity)	98%	0.34/h	-	1.2-2/h, 0.6/h	0.15/h

[a]Including a wireless power supply generator, TX and stimulator
[b]Including an stimulator/channel and an UWB TX
[c]Including an UWB TX   [d]Active area (excluding pads)