A 25Gbps 3D-Integrated CMOS/Silicon Photonic Optical Receiver with -15dBm Sensitivity and 0.17pJ/bit Energy Efficiency

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With continuous demand for higher bandwidth chip-to-chip communication, signaling over wires has become extremely challenging [1]. Optical signaling is an attractive alternative due to its small frequency-dependent loss and higher bandwidth. Recent advances in silicon photonic devices and 3D integration [2] have enabled them to be a viable solution for dense chip-to-chip interconnection. A key design metric for interconnects is the link power efficiency at a specific distance. In a modulator-based optical link, power is dissipated not only in the electronic circuitry, but also in the laser source. Improving the sensitivity of the receiver, which translates to lower laser power, can significantly reduce the power consumption of the link. In this work, a highly sensitive receiver topology is presented that is suitable for ultra-low capacitance front-ends. Low capacitance has become feasible by 3D integration of CMOS chip with a silicon-photonic (SiPh) chip containing a waveguide-coupled photodiode. The 3D integration is based on Copper Pillar (CuP) flip-chip bonding that enables low parasitic capacitance and dense interconnections with the SiPh (40µm pitch). For comparison purposes two CMOS receivers are integrated with the same SiPh chip. Both prototypes are fabricated in a 28nm CMOS technology as shown in Fig. 1. The first design shown in Fig. 1 (a) is an integrating receiver with a low bandwidth (LBW) TIA front-end [3]. The second design, shown in Fig. 1 (b), is a 3-stage conventional TIA architecture similar to [4].

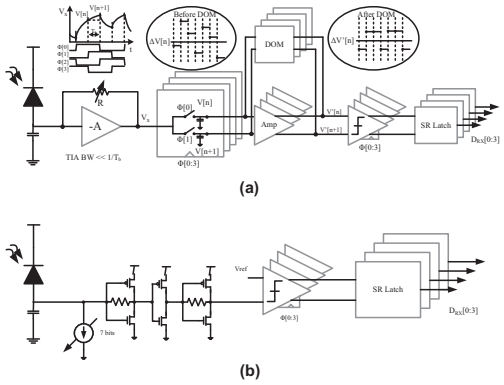

Fig. 1. (a) Double-sampling Rx with LBW TIA front-end. (b) Rx based on 3-stage inverter based TIA.

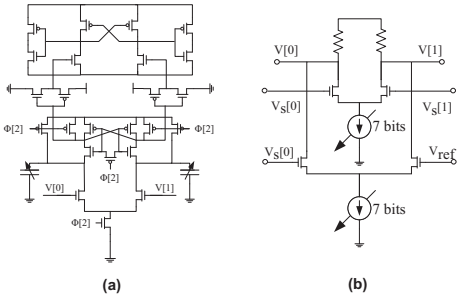

Fig. 2. (a) Sense-amp and SR latch used in both Rx designs (b) Differential pairs used for isolating amplifier and DOM.

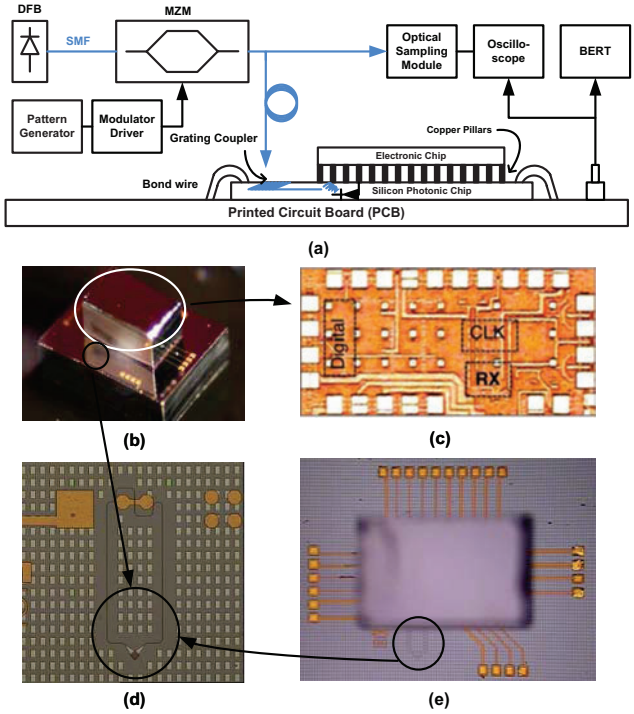

Fig. 3. (a) Test setup (b) 3D integrated (CMOS/ SiP) optical receiver (c) CMOS chip micrograph (d) grating coupler/ polarization splitter (e) top view micrograph of 3D integrated receiver.

A conventional optical receiver relies on full-bandwidth, determined by bitrate, of the TIA front-end and following gain stages [4], [5]. An integrating receiver, on the other hand, compares the signal level at the beginning and end of bit time interval and does not need the full-bandwidth [3]. In the integrating receiver architecture, a LBW TIA is placed between sampling capacitors and the front-end capacitor, providing isolation between PD's capacitor and sampling capacitors, which reduces charge-sharing effect and enables use of ultra-low capacitance photo-detectors in silicon photonic. With addition of LBW TIA, for a given PD capacitance, S/H capacitors can be chosen to be bigger (even comparable to PD's capacitance) to relieve KT/C noise thus enhancing the sensitivity of receiver. Fig. 2 shows circuit design details of the sense-amp and SR latch common to both designs, as well as the differential pairs used as amplifiers and DOM.

Fig. 3 (a) shows the measurement setup. CMOS receivers were bonded to a SiPh chip with ultra-low capacitance CuP flip-chip process. The SiPh chip has a grating coupler to couple light from an off-chip source, polarization splitter and two waveguides that carry the optical data to the PD. The total capacitance due to the photodiode, CuP bonds and pad is estimated to be less than 15fF. The optical beam from a 1550nm DFB laser diode is modulated by a high-speed Mach-Zehnder modulator and coupled to the photodiode through a single-mode fiber. The PD responsivity including grating coupler losses was measured to be 0.2A/W. Fig. 3 (b)-(e) show the 3D integration of electronics/photonics as well as the top view of CMOS and SiPh chips.

The receivers were tested using PRBS 15 sequence. Fig. 4 shows how sensitivity of the receivers changes with data rate. The coupling loss (measured to be 6dB) is included in this plot. For bit-error rate (BER) of 10^{-12}, the conventional receiver requires -10.4dBm of optical modulated amplitude (OMA) at 21.2Gb/s (its maximum speed), while the integrating architecture requires OMA of -16.1dBm at 21.2Gb/s and -14.9dBm at 25Gb/s.

The receivers' power consumption and energy efficiency at different data rates are shown in Fig. 5. In both designs, the power of digital elements increases linearly with speed. The 3-stage TIA design offers per-bit energy consumption of 226 fJ/bit at 21.2Gb/s compared with the integrating architecture that has per-bit energy consumption of 171fJ/bit at 21.2Gb/s. Energy efficiency of the integrating design reaches its peak of 170fJ/bit at 25Gb/s. Fig. 6 shows bath-tub curves of receiver designs at their respective maximum operational speeds.

The integrating receiver provides high sensitivity while maintaining low power consumption. This architecture is well suited for 3D integrated silicon photonic and CMOS technologies with ultra-low capacitance. Experimental results validated the feasibility of the receiver as well as its superiority over conventional TIA architecture in terms of power consumption, sensitivity and speed.

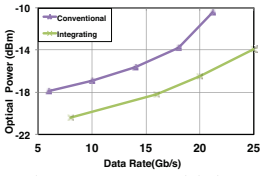

Fig. 4. Rx sensitivity at different data-rates.

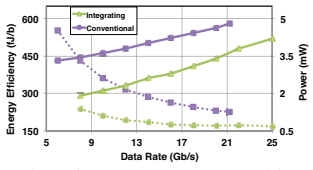

Fig. 5. Rx energy per bit (dashed) and power (solid).

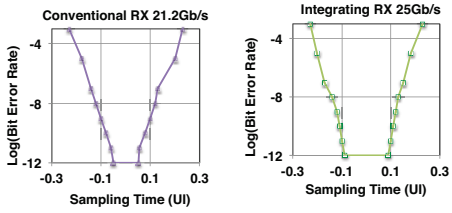

Fig. 6. Bath-tub curves for conventional and integrating receivers at 21.2Gb/s and 25Gb/s.

References

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