An 8 GHz First-Order Frequency Synthesizer for Low-Power On-Chip Clock Generation

Saman Saeedi, *Student Member, IEEE*, and Azita Emami-Neyestanak, *Member, IEEE*

***Abstract*—This paper presents a low-power first-order frequency synthesizer architecture suitable for high-speed on-chip clock generation. The proposed design features an architecture combining an *LC* quadrature voltage-controlled oscillator (VCO), two sample-and-holds, a phase interpolator, digital coarse-tuning and rotational frequency detection for fine-tuning. Similar to multiplying delay-locked loops (MDLLs), this architecture limits jitter accumulation to one reference cycle, as jitter during one reference cycle does not contribute to the next reference cycles. Also, instead of using multiplexer switches commonly employed in MDLLs, the reference clock edge is injected by phase interpolation to support higher frequencies and lower jitter. Functionality of the frequency synthesizer is validated between 8–9.5 GHz, *LC* VCO's range of operation. First-order dynamic of the acquisition has been analyzed and demonstrated through measurement. The output clock at 8 GHz has an integrated rms jitter of 490 fs, peak-to-peak periodic jitter of 2.06 ps and total rms jitter of 680 fs. Different components of jitter have been analyzed and separate measurements have been done to support the analysis. The reference spurs are measured to be −64.3 dB below the carrier frequency. At 8 GHz the system consumes 2.49 mW from a 1 V supply.**

***Index Terms*—Clock generation, clock multiplier, frequency synthesizer, interpolation, phase-locked loop (PLL), quadrature.**

I. Introduction

FREQUENCY synthesizers have versatile application in on-chip clock generation. Frequency synthesizers in the form of frequency multipliers play a key role in design of high-speed serial links, shown in Fig. 1. As the aggregate bandwidth requirement for chip-to-chip interconnects grows, their respective frequency of operation increases [1]. Additionally, high-speed link's timing noise heavily depends on jitter performance of clock multiplier, which takes a low-jitter low-frequency reference and generates the high frequency clock for the transceivers.

Conventional multiplying phase-locked loop (MPLL) architecture, shown in Fig. 2(a), has been the dominant architecture in this field for many years [2]–[8]. PLLs are appealing for use as frequency synthesizers due to their low complexity and because their architecture can support a programmable multiplication rate. More recently, delay-locked loop (DLL)-based frequency synthesizers have been under exploration [9]–[15].

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The authors are with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: ssaeedi@caltech.edu).

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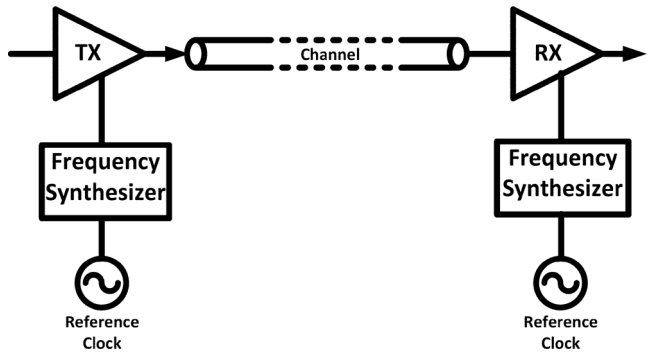

Fig. 1. Basic elements of a high-speed serial link.

A conventional MPLL exhibits higher jitter than a multiplying DLL (MDLL) with same building blocks and noise environment due to higher jitter accumulation [16]. In the MPLL of Fig. 2(a), a step variation in the phase of the ring oscillator gets integrated over many cycles until the loop filter can respond while it only causes a constant offset in a DLL. This results in a considerably larger peak phase error for a conventional PLL compared with DLL. Reducing jitter accumulation, which has motivated this work, is particularly important in systems with large digital switching noise where a clean reference is available. Prior to presenting the proposed architecture, we briefly review other clock multiplying architectures and particularly those that suppress jitter accumulation.

Fig. 2(b) shows a possible architecture for a DLL-based frequency synthesizer [13]. In this scheme, an edge-combining logic processes equal phases of the reference clock to produce higher frequency clock. As the reference clock is used to generate the output clock, with every new clock edge jitter from previous cycles is removed from output. Hence, this architecture limits jitter accumulation and does not rely on high loop bandwidth for jitter correction. On the other hand, this architecture has two primary drawbacks. Delay element nonidealities such as mismatch cause duty cycle distortion and a fixed-pattern jitter. Also, in this architecture it is difficult to achieve programmability for the required multiplication ratio. Fig. 2(c) shows another possible scheme for clock generation called multiplying DLL (MDLL) [9]. MDLL works by replacing the rising edge of the reference clock with the output clock in every reference cycle. With a clean reference, each rising edge of the reference clock zeros the phase error of the output. Therefore, jitter accumulation is limited to one reference clock period. Since a single delay element is used to generate the edges of output clock there is no fixed pattern jitter due to delay element mismatch. Besides,

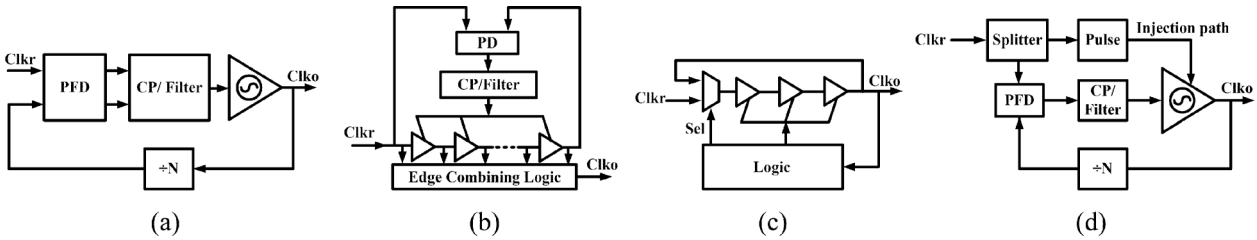

Fig. 2. Examples of prior art. (a) Conventional multiplying PLL (MPLL). (b) Edge-combining DLL-based frequency synthesizer. (c) MDLL. (d) Injection-locked-MPLL (IL-MPLL).

the select logic can be digitally controlled to program the multiplication rate. The logic block that generates a select pulse, which opens an aperture for reference injection, limits jitter performance and the maximum output frequency of MDLL. Recent works show how an aperture position tuning technique can enhance jitter performance of MDLLs and significantly reduce reference spurs [11], [5]. Also, there are other building blocks in MDLLs as well as MPLLs, such as phase frequency detector (PFD) and charge pump (CP), that impact their overall performance. Extensive work has gone through reducing power consumption of these building blocks, enhancing their speed and eliminate their sensitivity to device mismatch [2], [6], [17]–[23].

Note that, while suppressing jitter accumulation is important in frequency synthesizers, it is not necessarily the dominant source of jitter at the output of a frequency synthesizer. In case the reference clock itself has significant jitter, unlike MDLL, an MPLL can potentially filter out the reference clock jitter. More specifically, a PLL with a sufficiently narrow low-pass filter can filter high frequency components of the input noise. This is not always desirable as larger filter bandwidth results in better VCO noise filtering, faster settling time and smaller filter area. Other PLL-based frequency synthesizers such as subsampling PLLs [20], [24] and PLLs with dynamic phase error compensation [25] have been proposed to increase the loop bandwidth without compromising system performance.

Furthermore, there are other metrics that can be the bottleneck of frequency synthesizer's performance depending on the application. For example jitter peaking, which is the amplification of jitter transfer function over a certain frequency band, presents itself in conventional second-order PLLs with a closed loop zero. Jitter peaking in clock distribution networks with several cascaded PLLs or DLLs can cause significant performance degradation. Therefore, several techniques have been proposed to minimize or completely eliminate jitter peaking by removing the closed-loop zero [26], [27]. Note that jitter peaking is characterized by transfer function of reference to output while jitter accumulation can be described as how the output clock responds to noise on the control line of the VCO. [28] shows how certain types of MDLLs [e.g., Fig. 2(c)] suffer from jitter peaking while they exhibit jitter accumulation only during one reference period. Another class of frequency synthesizer architectures is those exploiting injection locking. Injection-locked PLLs (IL-PLLs) [shown in Fig. 2(d)], multiplying injection-locked oscillators (MILOs) are examples of such architecture. If the natural running frequency of the VCO is close to the Nth harmonic of the reference frequency, the VCO will lock to that harmonic such that output frequency becomes N times the reference frequency. There is a key difference between reference injection phenomena happening in MDLL and ILO-based frequency synthesizers. While having a clean reference an MDLL can completely clear jitter accumulation every reference cycle, in ILO-based frequency synthesizers reduction in jitter accumulation depends on injection strength and it reaches its peak when injected signal has the same frequency as the natural frequency of the oscillator [29]. Since PVT variations can deviate natural frequency of an oscillator from frequency of interest, injection locking may occur at the edge of the locking range with marginal reduction in jitter accumulation [29]. For effective injection locking, the VCO's natural frequency must be kept very close to the Nth harmonic of the reference clock. Therefore, a separate loop is necessary to adjust the VCO's natural frequency [30], [31].

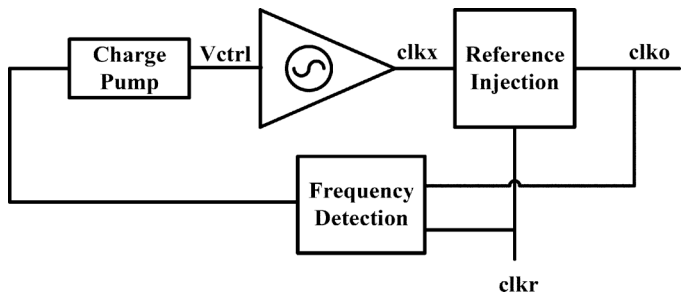

Fig. 3. Proposed first-order frequency synthesizer.

An alternative approach for reduction of jitter accumulation is presented in this paper; see Fig. 3 [32]. This architecture directly injects the rising edge of the reference clock to the output clock, resetting jitter accumulation similar to an MDLL. Also, first-order frequency detection and frequency correction is used, providing unconditional stability. The first-order frequency synthesizer architecture, shown with more details in Fig. 4, provides programmable clock multiplication with reduced jitter accumulation compared with conventional PLLs and without challenges in producing a select signal for open aperture in a multiplying DLL [9], [12]. This architecture utilizes a phase-interpolator (PI) based reference injection proposed in [34] for a burst-mode CDR application. PI-based reference injection, provides high-frequency feed-forward reference injection without using a MUX as in MDLLs [12]. In contrast to ILO-based reference injection, in the PI-based reference injection jitter accumulation suppression does not degrade as reference deviates from the VCO's natural frequency (the output rising edge is effectively replaced with the reference rising edge). Also, unlike MDLLs, the proposed

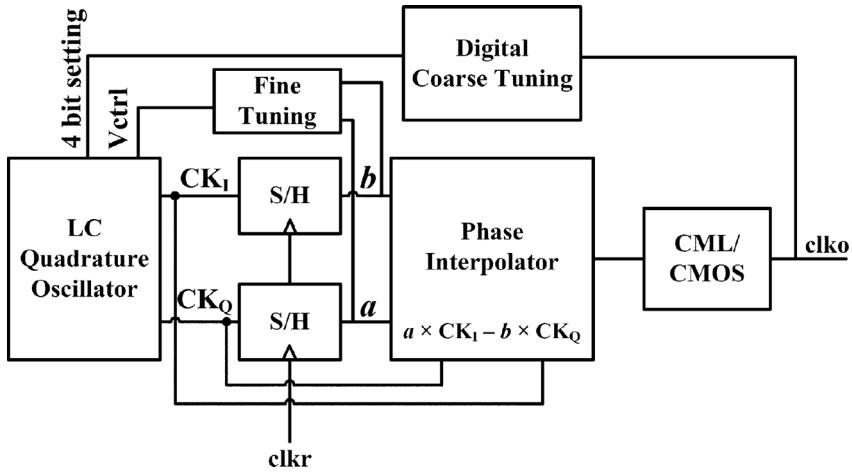

Fig. 4. Top-level architecture of the first-order frequency synthesizer.

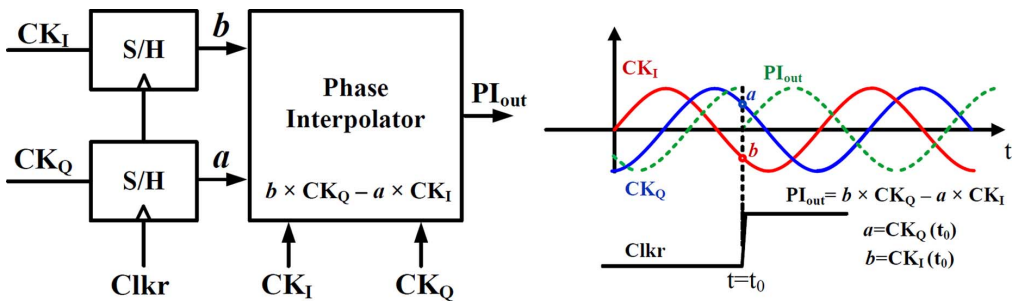

Fig. 5. Principle of phase-interpolation based reference injection.

architecture can utilize both an *LC* oscillator and inverter-based ring oscillator, depending on application and jitter requirements. In the prototype presented in this paper, an *LC* VCO has been used for low phase-noise demonstration. Frequency acquisition is achieved by a low-power implementation of rotational frequency detector [33], in conjunction with a digital coarse-tuning. Reference of the proposed architecture must be kept very clean since any jitter on this signal will pass directly to the output. Since the performance of this frequency synthesizer is highly dependent on the quality of the reference clock, in addition to electrical reference clock, as an extra feature, the prototype chip is capable of receiving a low jitter optical reference clock generated by a high-repetition-rate mode-locked laser [35]. Also, any nonlinearity in the design of reference injection causes a systematic jitter at the output clock. Therefore, careful attention to the design of the sample-and-holds and phase-interpolator for reference injection is required. The proposed frequency synthesizer is implemented in a 65-nm CMOS technology. It operates with a reference clock in the range of 400 MHz to 1 GHz to generate an output signal in the range of 8–9.5 GHz. The frequency synthesizer can be programmed to multiply the frequency by any value between 8–24, as long as the reference clock frequency and output clock frequency fall within ranges mentioned above. The prototype is fully tested with electrical reference clock and its performance is measured. This paper is organized as follows. Section II explains the overall system architecture and principles of operation and explains the mathematical principles of operation for this architecture. Section III explains circuit implementation details. Section IV covers analysis and supporting measurement. Finally, Section V is the summary and conclusion of the paper.

II. System Architecture and Principles of Operation

The basic operation of this system can be broken into three main elements. The reference clock injection restarts the phase at every rising edge of the reference clock, and will make the output clock phase independent of the VCO phase (the effect of circuit nonidealities will be discussed later in Section IV). The coarse-tuning forces the output clock to have exactly M rising edges in one reference clock period, and the fine-tuning, which has first order dynamics tunes the output frequency to be exactly M times the input frequency. First, we explain the operation of PI-based reference injection. Then, the algorithm for digital coarse tuning is discussed. Finally, details of fine-tuning rotational frequency detection is explained. The PI-based reference injection technique is shown in Fig. 5. The quadrature clocks ($\mathrm{CK_I}$ and $\mathrm{CK_Q}$), with arbitrary phase of ϕ_0 are sampled at the rising edges of the reference clock (b and a). These samples are then used to interpolate between $\mathrm{CK_I}$ and $\mathrm{CK_Q}$ using the phase interpolator. A reference clock rising edge at t_0 results in an output with zero crossing at t_0, regardless of the absolute phase of $\mathrm{CK_I}$ and $\mathrm{CK_Q}$ (Fig. 5):

$$a = \mathrm{CK_Q}(t_0) = -\cos(2\pi f t_0 + \phi_0) \quad (1)$$

$$b = \mathrm{CK_I}(t_0) = \sin(2\pi f t_0 + \phi_0) \quad (2)$$

$$PI_{\mathrm{out}} = b \times \mathrm{CK_Q} - a \times \mathrm{CK_I} = \sin(2\pi f(t - t_0)). \quad (3)$$

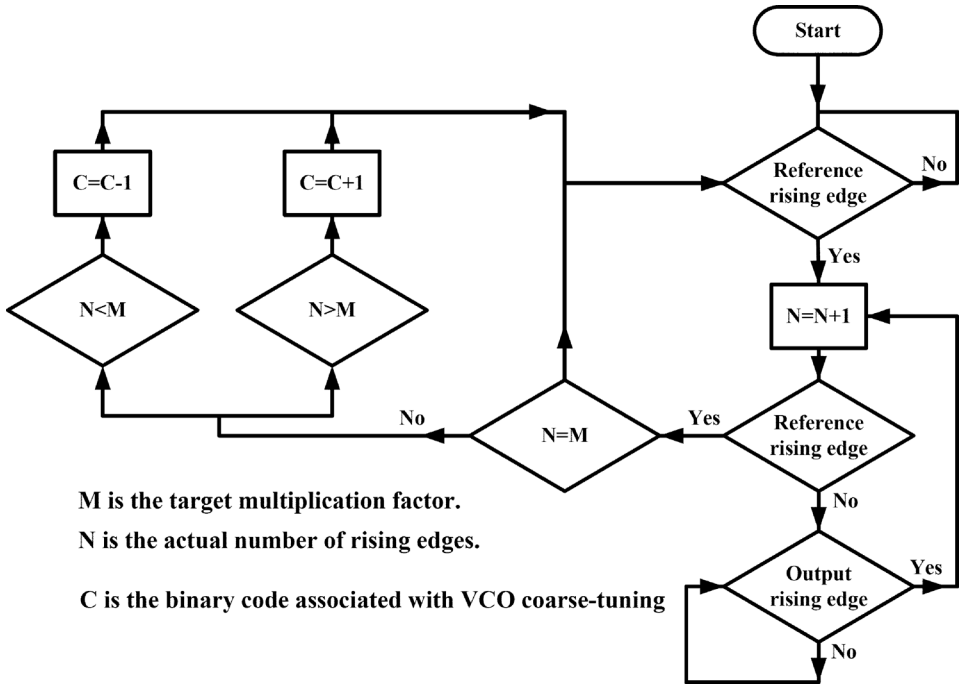

Fig. 6. Digital coarse-tuning flow chart.

This technique has been previously used in implementation of a burst-mode CDR [34].

Reference injection resets any unwanted noise event on VCO node on the next reference cycle. Furthermore, it clears low-frequency components of the VCO phase noise by injecting the reference to the output.

The flow chart in Fig. 6 demonstrates the operation of the coarse-tuning block. The primary function of the coarse-tuning block is to make the frequency synthesizer programmable and increase its locking range. The coarse-tuning block is a low-power digital circuit, comprising two counters and two comparators. It counts the number of rising edges of output clock in each reference clock period, and compares it to the target multiplication factor. The output of the comparator changes a 4-bit word that controls part of the capacitance of the quadrature LC VCO, adjusting its frequency of operation. Since the phase interpolator injects the rising edge of the reference, VCO's output can have the same number of rising edges for a range of input frequencies. The coarse-tuning procedure works throughout acquisition, and as soon as the target multiplication rate is achieved, coarse-tuning binary code is fixed. A separate block fine-tunes the VCO's frequency with an additional varactor. While the fine-tuning is active, the number of rising edges within one reference period remains constant. Therefore, coarse tuning makes no corrections after the binary code is fixed. During the few cycles that the coarse-tuning sets the binary code, the fine-tuning corrections are negligible (due to the small loop gain of fine-tuning).

The basic idea of a fine-tuning frequency detector, known as a rotational frequency detector [33], is shown in Fig. 7. Following is a brief explanation of the concept. The input of the fine-tuning block is same samples taken for interpolation (a and b). Its output is UP and DN bang-bang pulses for a charge-pump that corrects control voltage of the quadrature *LC* VCO. The following equations describe the nth sample taken from $\mathrm{CK_I}$ and $\mathrm{CK_Q}$ as follows:

$$\mathrm{CK_{I,S}} = \cos(2\pi f_{\mathrm{VCO}} t_n + \phi_0) \tag{4}$$

$$\mathrm{CK_{Q,S}} = \sin(2\pi f_{\mathrm{VCO}} t_n + \phi_0). \tag{5}$$

where t_n is when the nth sample is taken, ϕ_0 is the arbitrary phase of the VCO output, and f_{VCO} is the VCO oscillation frequency. t_n is defined as

$$t_n = \frac{n}{f_{\mathrm{ref}}} \tag{6}$$

$$f_{\mathrm{VCO}} = M f_{\mathrm{ref}} \pm \Delta f \tag{7}$$

where Δf is the frequency error of the *LC* VCO. Plugging (6) and (7) into (4) and (5), we obtain

$$\begin{aligned}\mathrm{CK_{I,S}} &= \cos\left(2\pi M n \pm \frac{2\pi n \Delta f}{f_{\mathrm{ref}}} + \phi_0\right) \\ &= \cos\left(\frac{2\pi n \Delta f}{f_{\mathrm{ref}}} + \phi_0\right)\end{aligned} \tag{8}$$

$$\begin{aligned}\mathrm{CK_{Q,S}} &= \sin\left(2\pi M n \pm \frac{2\pi n \Delta f}{f_{\mathrm{ref}}} + \phi_0\right) \\ &= \sin\left(\pm\frac{2\pi n \Delta f}{f_{\mathrm{ref}}} + \phi_0\right) \\ &= \cos\left(\frac{2\pi n \Delta f}{f_{\mathrm{ref}}} + \phi_0 \pm \frac{\pi}{2}\right)\end{aligned} \tag{9}$$

describing frequency and phase relationship of the samples.

As can be seen in Fig. 7, the frequency of $\mathrm{CK_{I,S}}$ and $\mathrm{CK_{Q,S}}$ is analogous to the beat frequency of two interfering waveforms

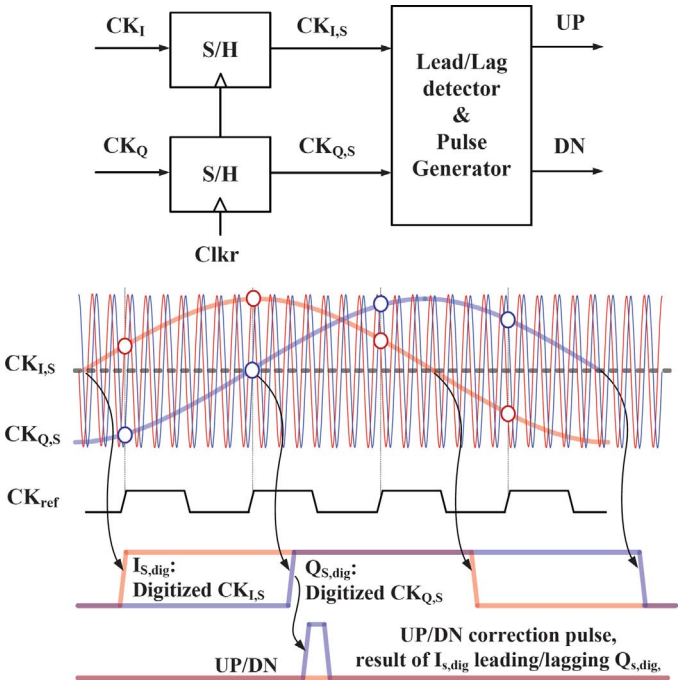

Fig. 7. Principle of beat frequency in fine-tuning frequency detection.

with slightly different frequencies. This frequency is proportional to frequency error of the VCO:

$$f_{\text{beat}} = f_{\text{CK}_{\text{I,S}}} = f_{\text{CK}_{\text{Q,S}}} = |f_{\text{VCO}} - M f_{\text{ref}}|. \quad (10)$$

The absolute phase difference between $\text{CK}_{\text{I,S}}$ and $\text{CK}_{\text{Q,S}}$ waveforms is always $\pi/2$. The sign of frequency error determines which one of $\text{CK}_{\text{I,S}}$ and $\text{CK}_{\text{Q,S}}$ leads the other one. As will be discussed in the subsequent sections, this property and (10) will be used to implement rotational frequency acquisition.

III. Circuit Implementation

Fig. 8 shows the transistor-level implementation of the main building blocks. Fig. 8(a) shows the quadrature oscillator used in the system with four coarse-tuning bits and fine-tuning control voltage. The quadrature *LC* VCO is implemented by two matched *LC* VCOs that are coupled in a quadrature VCO (QVCO) configuration. Antiphase coupling is achieved using pMOS differential pairs. The *LC* tank's natural frequency is varied by 4 bits of digital coarse tuning connected to four varators and one analog voltage connected to a fifth varactor. Varactors are made of a pair of nMOS transistors in accumulation mode. Fig. 8(b) shows the master–slave S/H implementation. The master-slave S/H comprises of two pass transistors, two transmission gates and a differential buffer with source degeneration between them. The pass transistors and transmission gates act as track-and-hold elements that are triggered opposite edges of the reference clock. While the pass transistors hold the voltage levels in parasitic capacitors of the next stage at rising edge, the transmission gates keep the voltage as the reference clock voltage falls. The buffer with source degeneration is used to minimize kickback [36] and charge-sharing from the output transmission gates to the input pass gates [34]. Nonlinearity of S/H induces jitter at the output of the phase-interpolator. Source degeneration in the buffer ensures this systematic jitter is minimized [37]. The pass-transistor is sized to minimize reference charge injection thus spurs in the output clock. The S/H is optimized to have maximum bandwidth and linearity. Fig. 8(c) shows the differential phase interpolator architecture. The interpolation coefficients (a and b) are converted from voltage to current using a differential transconductance stage. The operation of interpolation is performed in current mode and is converted to voltage at output nodes with resistors. Clock samples as well as quadrature waveforms are differential to minimize supply noise and phase mismatches.

The circuit implementation of the bang-bang rotational frequency detector is shown in Fig. 9. The fine-tuning circuit uses the beat frequency to set the correction rate proportional to the frequency error and phase relationship between the signals. The principle of fine-tuning is based on the beat frequency and phase difference of samples taken from CK_{I} and CK_{Q}. These samples have the beat frequency described in (10). In this design D flip-flops are used to determine the phase relationship between $\text{CK}_{\text{I\_S}}$ and $\text{CK}_{\text{Q\_S}}$. By extracting the phase information of $\text{CK}_{\text{I,S}}$ and $\text{CK}_{\text{Q,S}}$, bang-bang UP/DN pulses associated with each case are generated to increase and decrease the fine-tuning control voltage of LC quadrature VCO. The frequency acquisition behaves as a first order system since corrections are proportional to deviation of output frequency from M times frequency of the reference clock. Schmitt triggers are used to prevent metastability and unwanted pulses when frequency of oscillator is close to M times frequency of the reference clock. Note that, unlike conventional PFDs, where UP/DN signals turn on at the same time, in this frequency detector UP/DN signals are independent.

Fig. 10 shows electrical/optical reference generator. A MUX chooses between the two signals. The electrical reference generator, which is used during the test, is simply a CML/CMOS circuit retrieving the signal from an off-chip source. As an additional feature, the chip can also use optical reference. The optical reference generates sharp rising edges from high-repetition rate mode-locked laser. A tunable feedback circuit resets the voltage before the next pulse arrives. An on-chip tunable RC delay controls the duty-cycle of the reference waveform. Since only the rising edge of the reference is injected to the output clock the duty-cycle and jitter of the falling edge do not play a role in the quality of the output clock.

IV. Analysis and Measurements

The proposed frequency synthesizer is fabricated in 65 nm CMOS technology. Fig. 11 shows real-time acquisition of the system at 8 GHz while locking to a 400 MHz reference clock. As coarse-tuning and fine-tuning loops correct the frequency of the generated clock, the operation of the reference injection can be seen at three different time steps. While the rising edge is always injected with the same relative phase, frequency of the quadrature VCO changes until lock is acquired. The frequency synthesizer has an operating range of 8–9.5 GHz limited by the *LC* VCO's frequency range.

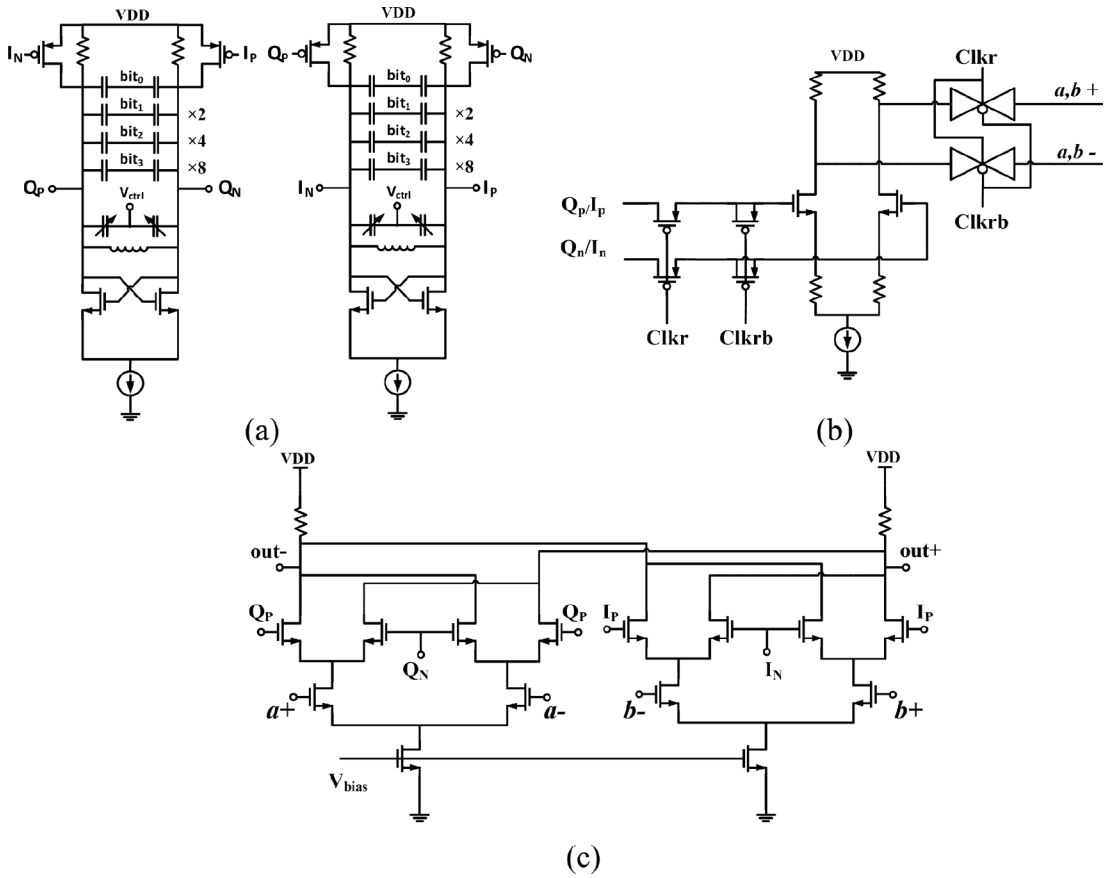

Fig. 8. Transistor-level schematics of main building blocks. (a) *LC* quadrature VCO. (b) Master–slave S/H. (c) Differential phase-interpolator.

Fig. 12(a) shows reference spurs that are measured to be 64.3 dB lower than the main carrier frequency. The overall jitter seen during measurement of the proposed frequency synthesizer can be separated to jitter due to device noise and jitter due to nonlinearity of different components

$$\sigma_{\text{total}}{}^2 = \sigma_{\text{random}}{}^2 + \sigma_{\text{systematic}}{}^2 \tag{11}$$

where σ_{random} is the variance of a normal Gaussian distribution of phase errors that is the result of the circuit and system thermal and device noises. The $\sigma_{\text{systematic}}$ is the rms of the systematic phase errors due to non-linearity of phase interpolator and S/H, phase mismatch in quadrature *LC* VCO, jitter due to loop dynamics and bang-bang frequency correction error. In order to test the chip, a clean reference clock, generated by signal generator, is divided by a power splitter. One output of the power splitter is used to trigger real-time oscilloscope and the other output is used as the reference for the test chip. Fig. 12(b) and (c) shows absolute jitter measurements, obtained by triggering the oscilloscope with the clean reference and measuring the phase jitter of the output clock. Fig. 12(b) shows the histogram and total peak-to-peak jitter of the system to be 9 ps and total rms jitter to be 680 fs. A real-time scope can distinguish Gaussian random jitter from the rest of jitter components. Fig. 12(c) shows the measured breakdown of the jitter performance. The output clock has a random rms jitter of 490 fs and the periodic peak-to-peak jitter is measured to be 2.06 ps. Fig. 12(d) shows phase-noise measurements indicating -127 dBc/Hz of phase noise at 1 MHz offset. For the same reference frequency of 400 MHz, jitter for three other multiplication factors (21, 22, and 23) have also been measured and shown in Fig. 13.

In order to characterize different components of jitter, different test-structures on the chip have been measured separately to show different jitter contributions. Fig. 14(a)–(d) shows simulation and measurement results of the quadrature *LC* VCO test-structure in room temperature. When the temperature is increased to 125°C, the simulated resonance frequency of the *LC* tank changes by less than 3.5%. The coarse-tuning range and steps are shown in Fig. 14(d). The fine-tuning simulation verifies a range between 420–510 MHz depending on frequency of operation. The bang-bang frequency corrections have steps of 1.6 MHz-2.5 MHz.

Phase noise of the open-loop oscillator is measured to be -91.8 dBc/Hz at 1 MHz offset. The maximum quadrature phase mismatch of the quadrature *LC* VCO is measured to be 2.7%. This quadrature phase error appears both on phase-interpolator coefficients (a and b) and corresponding clocks. For sufficiently small phase mismatch ($\Delta t \ll 1/f_{\text{ref}}$), the output amplitude error remains small, and the subsequent CML-to-CMOS stage removes any amplitude degradation. Also, the quadrature phase error has no effect on zero-crossing and therefore systematic

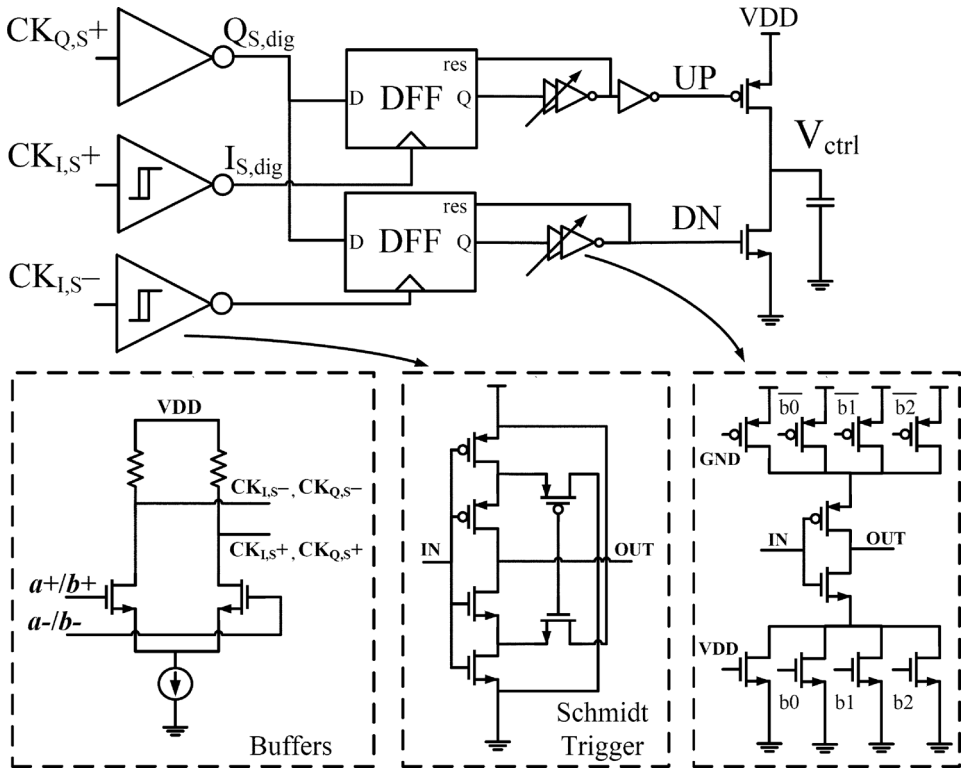

Fig. 9. Details of fine-tuning frequency-detection.

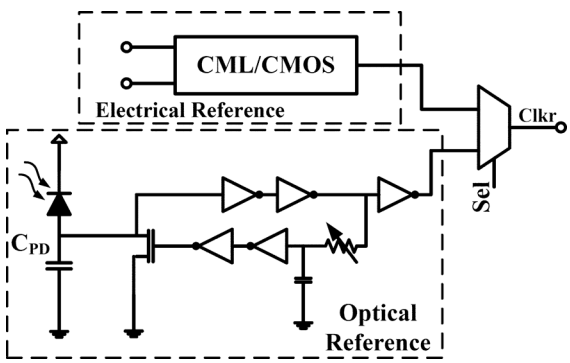

Fig. 10. Electrical/optical reference generator.

jitter of the output of the phase-interpolator. These conditions are shown as follows:

$$\begin{aligned} PI_{\text{out}}(t) &= b_{er} \times \text{CK}_{\text{Q}}(t) - a \times \text{CK}_{\text{I,er}}(t) \\ &= \sin\left(2\pi f(t_0 - \Delta t)\right)\cos(2\pi f t) \\ &\quad - \cos(2\pi f t_0)\sin\left(2\pi f(t - \Delta t)\right) \\ &= \cos(2\pi f \Delta t)\sin\left(2\pi f(t - t_0)\right) \\ &\approx \sin\left(2\pi f(t - t_0)\right) \qquad (12) \\ PI_{\text{out}}(t_0) &= \cos(2\pi f \Delta t)\sin\left(2\pi f(t_0 - t_0)\right) = 0. \qquad (13) \end{aligned}$$

A similar argument can be used to show that amplitude mismatch in the quadrature *LC* VCO does not affect the performance of phase interpolation either, as it appears in both the samples and the quadrature waveform as follows:

$$\begin{aligned} PI_{\text{out}}(t) &= b_{er} \times \text{CK}_{\text{Q}}(t) - a \times \text{CK}_{\text{I,er}}(t) \\ &= A_{I,\text{err}}\sin(2\pi f t_0) A_Q \cos(2\pi f t) \\ &\quad - A_Q \cos(2\pi f t_0) A_{I,\text{err}} \sin(2\pi f t) \\ &= A_{I,\text{err}} A_Q \sin(2\pi f(t - t_0)). \qquad (14) \end{aligned}$$

The quadrature phase mismatch (ϕ_{er}) of the LC VCO output translates to quadrature phase mismatch of the samples taken from CK_{I} and CK_{Q}:

$$\begin{aligned} CK_{I,S} &= \cos(2\pi f_{\text{VCO}} t_n + \phi_0) \\ &= \cos\left(\frac{2\pi n \Delta f}{f_{\text{ref}}} + \phi_0\right) \qquad (15) \\ \text{CK}_{\text{Q,S,er}} &= \sin(2\pi f_{\text{VCO}} t_n + \phi_0 + \phi_{er}) \\ &= \cos\left(\frac{2\pi n \Delta f}{f_{\text{ref}}} + \phi_0 + \phi_{er} \pm \frac{\pi}{2}\right). \qquad (16) \end{aligned}$$

Also, any mismatch in the delay of $I_{\text{s,dig}}$ and $Q_{\text{S,dig}}$ and duty-cycle distortion (DCD) in their waveforms further degrades their quadrature characteristic required for operation of the fine-tuning. These non-idealities can be summed up in T_{er}, defined in

$$|T_{er}| = \left|\frac{\phi_{er}}{2\pi \times \Delta f}\right| + \left|\frac{\frac{1}{2} - D_I}{2\pi \times \Delta f}\right| + \left|\frac{\frac{1}{2} - D_Q}{2\pi \times \Delta f}\right| + |T_\Delta|. \quad (17)$$

D_{I} and D_{Q} are DCD of $\text{I}_{\text{s,dig}}$ and $Q_{\text{S,dig}}$ respectively and T_Δ is their delay mismatch. Fine-tuning can only operate as long

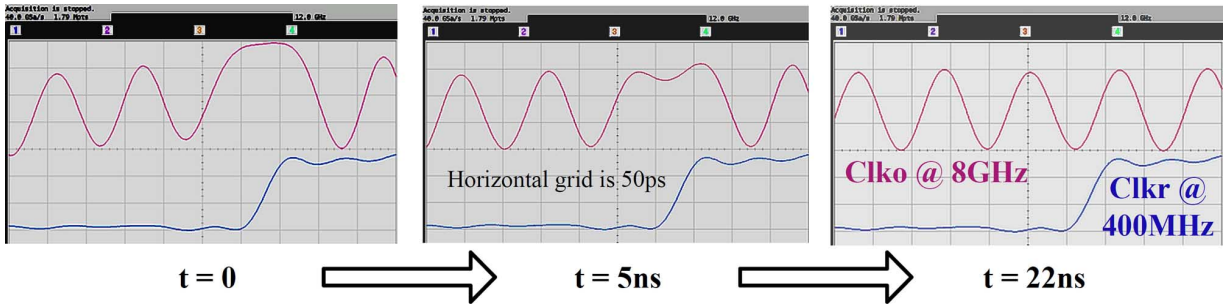

Fig. 11. Real-time acquisition for a reference clock of 400 MHz and output clock of 8 GHz.

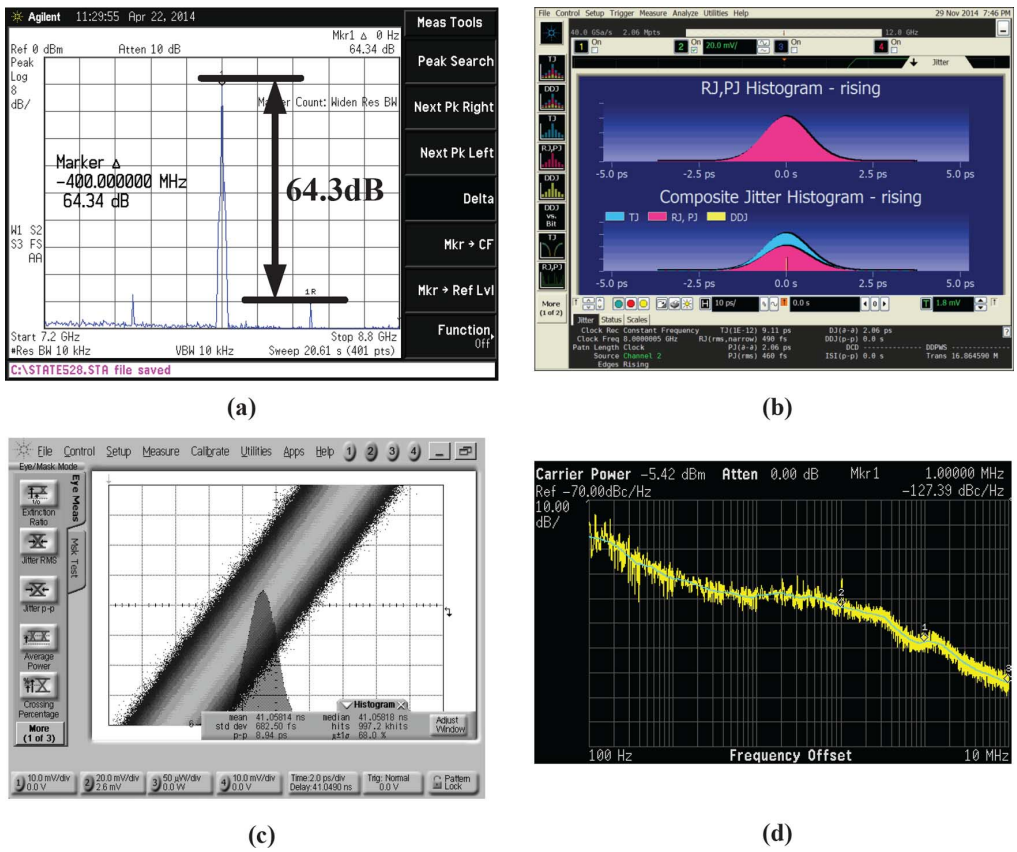

Fig. 12. (a) Measurement showing reference spurs at 8 GHz with 400 MHz reference. (b) Output clock jitter histograms. (c) Total jitter measurement. (d) Phase noise measurement.

as rising edges of $I_{\mathrm{s,dig}}$ and $Q_{\mathrm{S,dig}}$ (shown in Fig. 7) are distinguishable by flip-flops used in fine tuning Fig. 9. Distinguishability by flip-flops is determined by the following condition:

$$\frac{1}{4 \times |\Delta f|} - T_{er} > \max(t_{su,t_h}) \tag{18}$$

where t_{su} and t_h are setup time and hold time of the flip-flops. The maximum pull-in range is limited by the non-idealities of circuit implementation as described in (18). As the system gets close to lock and Δf gets smaller, time-domain difference between rising edges of $I_{\mathrm{s,dig}}$ and $Q_{\mathrm{S,dig}}$ gets easier to detect. The delay mismatch in UP/DN bang-bang pulses has no effect on the loop operation near lock as correction pulses are independent and do not rely on UP/DN overlap.

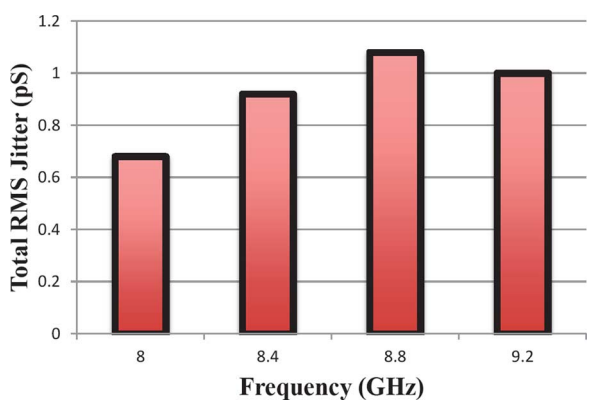

Fig. 13. Total rms jitter of output clock versus frequency.

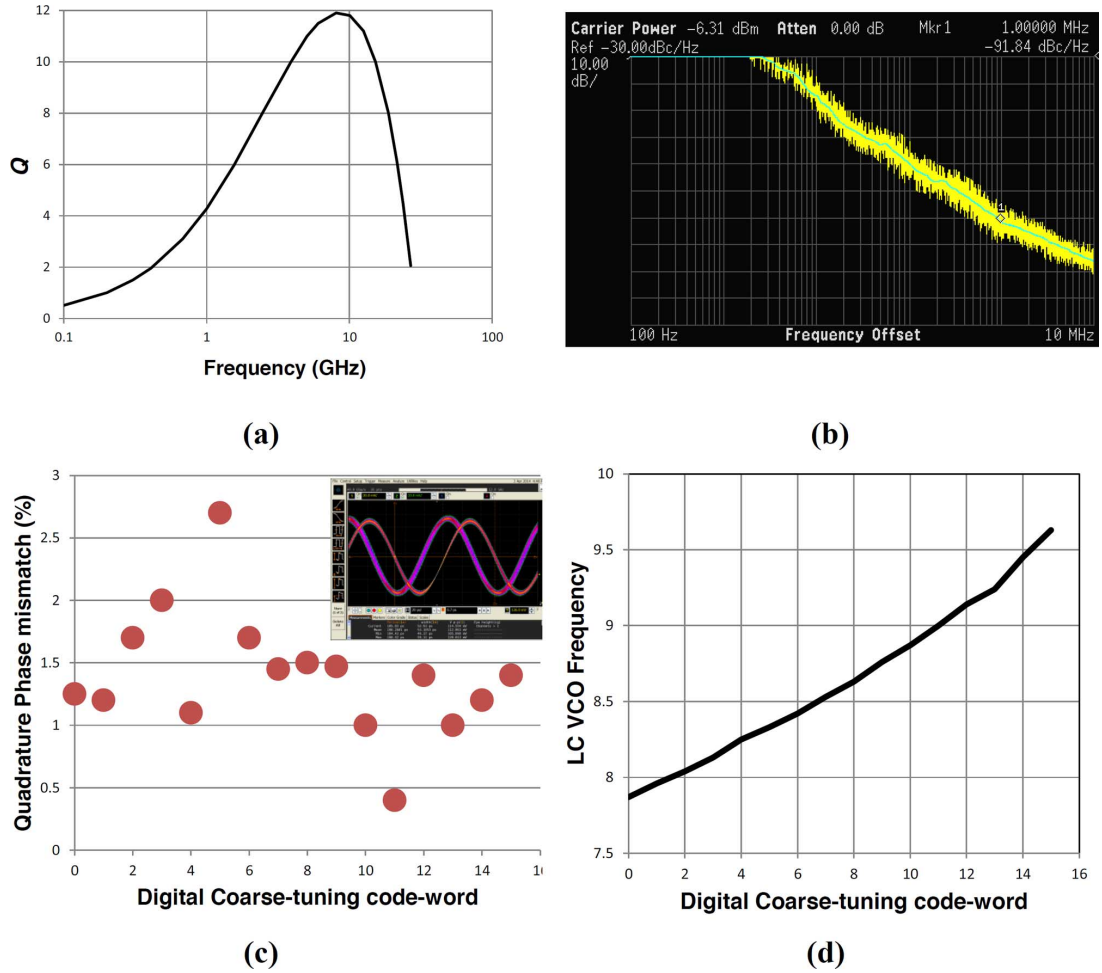

Fig. 14. Quadrature *LC* oscillator. (a) Simulated Q versus frequency. (b) Measured phase noise of open-loop *LC* VCO. (c) Quadrature phase mismatch. (d) Coarse-tuning code-word versus frequency.

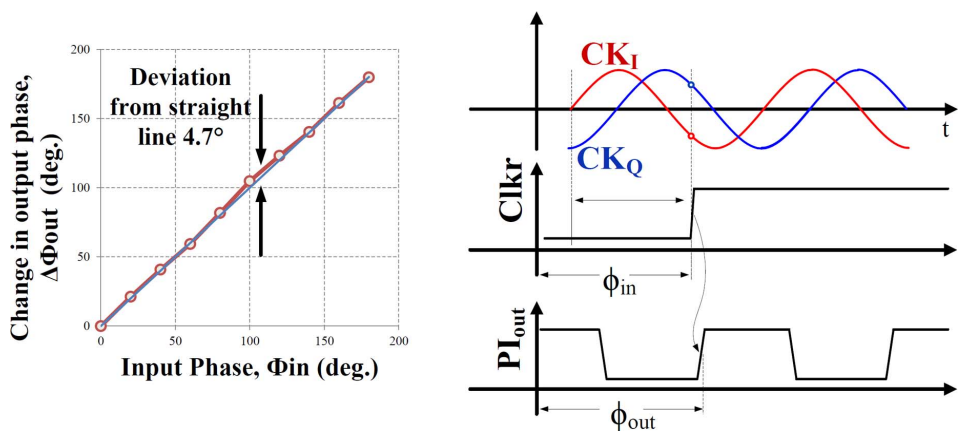

Fig. 15. Measured nonlinear characteristics of the S/H and PI.

Bang-bang UP/DN corrections of the fine-tuning block cause a small error in VCOs frequency. Note that as the rising edge of the reference is injected to the output, output clock will have zero average frequency error. However, as the injection occurs at a fraction of the VCO's frequency, error in VCO's frequency causes a periodic shift in the VCOs' phase compared with output phase, which leads to deterministic jitter and reference spurs. When the system is at lock, the difference between UP/DN pulses causes a frequency error $\Delta f_{\rm err}$. The periodic phase shift in VCO's phase compared with the output phase can be written as

$$\Delta T_{\rm err} = \frac{1}{f_{\rm ref}} - \frac{N}{N f_{\rm ref} - \Delta f_{\rm err}} \approx \frac{\Delta f_{\rm err}}{N f_{\rm ref}^2}. \qquad (19)$$

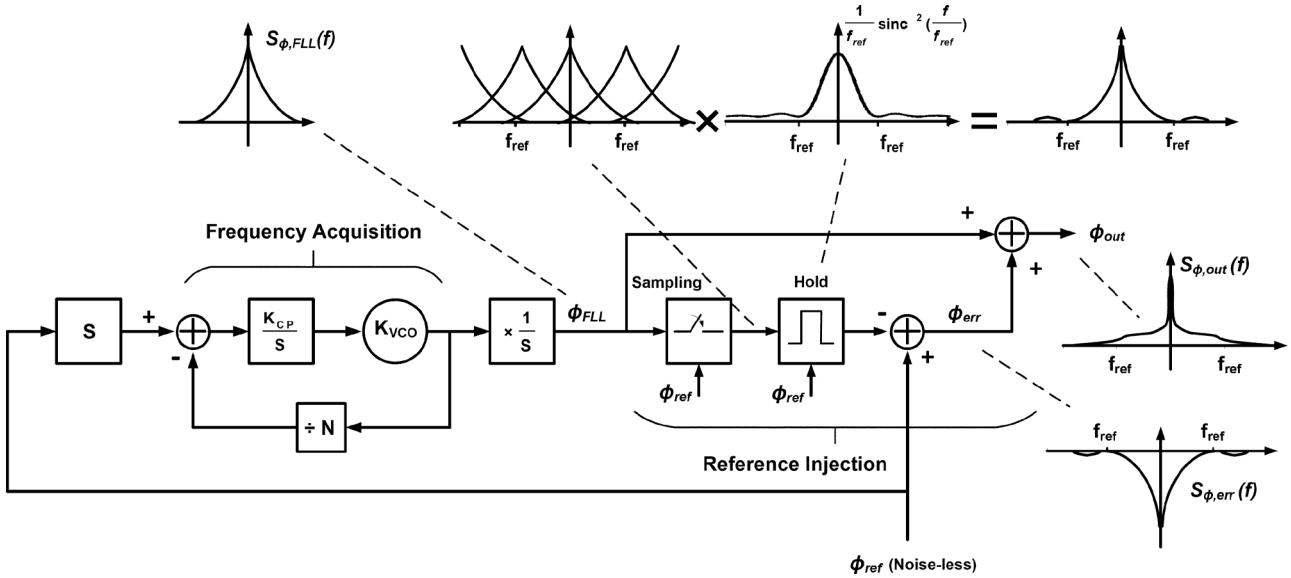

Fig. 16. Block diagram of the system and filtering of VCO phase noise in the presence of a clean reference.

Monte Carlo simulations show worst-case $\Delta f_{\rm err}$ to be around 0.5 MHz. From (19), for a multiplication factor of 20 and reference clock frequency of 400 MHz, $\Delta T_{\rm err}$ is 0.16 ps. This value of deterministic jitter gets larger with larger N or smaller reference frequency.

Fig. 15 shows measured non-linear characteristics of the S/H and phase interpolator. An off-chip reference clock and quadrature waveforms have been applied to a replica test structure that only contains phase interpolator and S/H. Shifting the relative phase of the reference and quadrature signals, the change in output phase has been measured. Maximum deviation from ideal line is measured to be 4.7°. This deviation means the output clock phase will not be completely independent of the VCO phase and the reference injection induces a systematic jitter. For an output clock of 8 GHz the peak-to-peak systematic jitter associated with this nonlinearity is 1.63 ps. As can be seen, the measured 2.06 ps periodic peak-to-peak jitter is largely associated with this nonlinear effect.

Fig. 16 shows the block diagram of the system including frequency acquisition and reference injection and the effect of reference injection on phase noise in the simplified case of noiseless reference. The system is modeled when the coarse-tuning code word is settled and system is within fine-tuning acquisition range. First, we will investigate the effect of reference injection on filtering the phase noise of the frequency-locked loop (FLL). Reference injection is modeled as shifting the phase of the FLL output by the difference between periodic samples of the FLL output phase and reference clock phase. In the frequency domain, this translates to convolution of an impulse train with the phase noise spectrum of the FLL output followed by a sinc function, shown as

$$\begin{aligned}\phi_{\rm out}(j\omega) &= \phi_{\rm FLL}(j\omega) + \phi_{\rm err}(j\omega)\\ &= \phi_{\rm FLL}(j\omega) - \left\{\sum_{k=-\infty}^{k=\infty} \phi_{\rm FLL}\left(j\omega - \frac{2\pi k}{T_{\rm ref}}\right)\right\}\\ &\quad \times T_{\rm ref}{\rm sinc}\big(T_{\rm ref}(j\omega)\big). \qquad (20)\end{aligned}$$

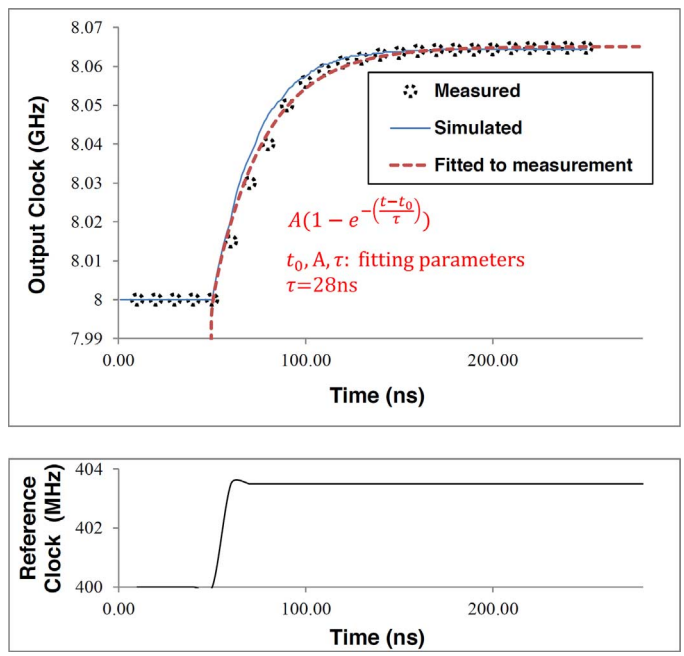

Fig. 17. Loop response measured by applying a step frequency to the reference clock.

Due to shape of the sinc function, reference injection filters out most of the low-frequency components of the noise (Fig. 16).

Another interesting case is when the reference is not clean. In that case there is a direct path for reference noise to appear at the output. The impulse train, by which the FLL output noise is convolved, will have the corresponding jitter and the sinc function will also be distorted depending on the shape of the reference clock's phase noise. Nonetheless, the low-frequency phase noise of the FLL output will still get filtered (now less effectively) as long as the reference jitter is small. In presence of a noisy reference, the FLL output will carry low-frequency components of the reference phase noise (high-frequency components get filtered out in the loop).

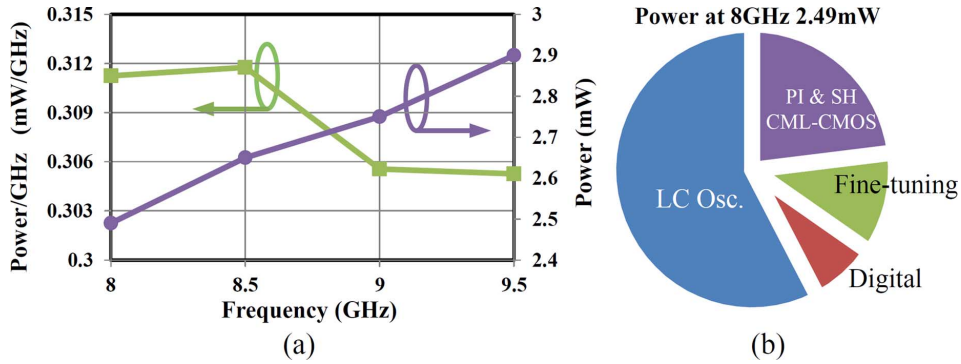

Fig. 18. (a) Power consumption and efficiency at different frequencies. (b) Power breakdown at 8 GHz.

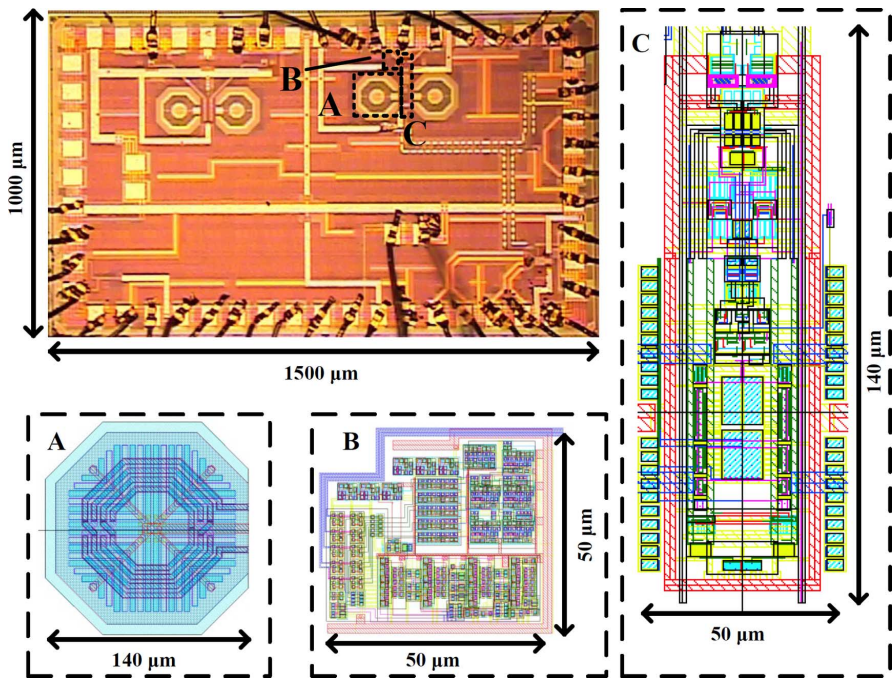

Fig. 19. Die micrograph and layout details of the implemented prototype. A. Design of inductor. B: Digital coarse-tuning block. C: Placement of the rest of the circuitry between the inductors.

The following equation shows the relation between reference clock and VCO frequencies:

$$\frac{f_{\mathrm{VCO}}}{f_{\mathrm{ref}}} = \frac{\frac{K_{\mathrm{CP}}}{s}K_{\mathrm{VCO}}}{1+\frac{\frac{K_{\mathrm{CP}}}{s}K_{\mathrm{VCO}}}{M}} = \frac{K_{\mathrm{CP}}K_{\mathrm{VCO}}}{s+\frac{K_{\mathrm{CP}}K_{\mathrm{VCO}}}{M}} = \frac{\omega_1}{s+\frac{\omega_1}{M}} \tag{21}$$

where M is the multiplication factor and ω_1/M represents the loop bandwidth.

In order to verify the loop dynamics of the system, a step frequency is applied to the reference changing the reference from 400 to 403.5 MHz. As the loop corrects the output frequency, the output clock is measured in real time and its frequency is measured over 300 ns. Fig. 17 shows the measured loop response, simulated loop response, and the curve fitted with the measurement results. The fitted first-order step response time constant is 28 ns (showing 5.7 MHz loop bandwidth). Fig. 18(a) shows the measured power consumption and energy efficiency of the frequency synthesizer while operating at different frequencies. Energy efficiency of the frequency synthesizer is 0.312 mW/GHz at 8 GHz, which drops to 0.305 mW/GHz at 9.5 GHz. As the frequency of operation increases, power consumption increases linearly primarily due to the power consumption of digital elements. The power consumption measurement includes *LC* quadrature oscillator, sample-and-holds, phase interpolator, coarse-tuning, fine-tuning, and output CML-to-CMOS converter. Fig. 18(b) shows the power breakdown of the frequency synthesizer at 8 GHz. More than half of the power is consumed by quadrature *LC* VCO.

Fig. 19 shows the chip micrograph. The frequency synthesizer occupies an active area of 0.044 mm^2 including the inductors. The octagonal structure of the inductor design, the digital coarse tuning block layout and placement of the rest of the circuits between the two inductors can also be seen in A, B, and C of Fig. 19, respectively. Table I summarizes performance of the frequency synthesizer and compares it with the state of

TABLE I
FREQUENCY SYNTHESIZER PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR ART

	This Work	[13]	[11]	[10]	[12]	[6]	[4]	[5]	[24]	[20]	[30]
Technology	65nm	.35µm	90nm	.13µm	90nm	32nm	40nm	65nm	.18µm	.13µm	90nm
Frequency [GHz]	8-9.5	0.9	1.6	1.5	4.6	26.7	5.83	1.6	2.2	3.2	20
Reference [MHz]	400-1000	100	50	375	395	400	26	40-300	55.25	50	1000
Reference Spurs [dBc]	-64.3	-30	-58.3	-55.6	-46	-96.3	-102	-40	-56	-63.9	-55
Integrated jitter/RMS[ps]	0.49	N/A	0.68	0.4	N/A	N/A	N/A	N/A	0.16	0.13	0.149
Total jitter RMS/PP [ps]	0.68*/9.11	N/A	N/A	0.9/9.2	2/17.8	N/A	0.3/-	0.7/-	N/A	N/A	N/A
Power [mW/GHz]	0.312	144	5.75	0.4	1.48	3.32	2.56	0.606	1.13	8.93	1.9
Area [mm^2]	0.044	1.2	0.76	0.25	0.025	N/A	0.29	0.022	0.2	0.4	0.325
Method	Proposed	DLL	MDLL	MDLL	MDLL	MPLL	MPLL	MDLL	SSPLL	PILO	ILPLL

* Represents 0.49 of integrated RMS jitter and 2.06ps of peak-to-peak periodic jitter

the art. While this table provides a glimpse at how different design topologies perform in terms of jitter, power, and reference spurs, the noise environment and reference quality plays an important role in final output jitter. The proposed architecture is a low-power alternative for on-chip frequency synthesizers limiting jitter accumulation to one reference period.

V. CONCLUSION

This paper presents a first-order frequency synthesizer. Injection of the rising edge of the clock limits jitter accumulation to one reference cycle, and first-order dynamic of the system ensures acquisition without stability concerns. Reference injection is implemented via phase-interpolation. The frequency acquisition consists of digital coarse-tuning and rotational frequency detection for fine-tuning. A prototype has been implemented in a 65 nm CMOS process, and has been fully verified via measurements and simulations. Experimental results validated functionality of the system with an electrical input clock. The total active area including inductors is 0.044 mm^2. The test chip operates in the range of 8–9.5 GHz. At 8 GHz, with a multiplication factor of 20, it consumes 2.49 mW, and exhibits 490 fs rms integrated jitter and 2.06 ps peak-to-peak periodic jitter. At this operating frequency, the reference spurs are measured to be 64.3 dB below the carrier frequency. The first-order characteristics of the frequency acquisition has been examined and demonstrated via measurement. Different factors contributing to the jitter have been analyzed and supporting measurements have been presented. This architecture is well suited for dense parallel links and noisy environments where a clean reference clock is available.

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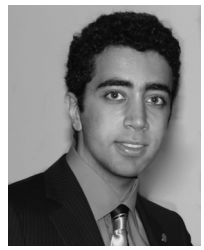

Saman Saeedi (S'14) received B.Sc. degree in electrical engineering and applied physics from Sharif University of Technology, Tehran, Iran, in 2010, and the M.S. degree in electrical engineering from California Institute of Technology, Pasadena, CA, USA, in 2011, where he is currently working toward the Ph.D. degree.

The focus of his current research is low-power, high-performance mixed-signal integrated circuits, with an emphasis on optical and electrical hybrid integration. During the summer of 2012, he was a Display Design Engineer with Apple Inc., where he worked on display driver chipsets. Since the summer of 2014, he has been with Rockley Photonics Inc., where he designs CMOS/silicon photonic high-speed optical links.

Mr. Saeedi was the recipient of the Gold Medal of the National Physics Olympiad and a four-year undergraduate fellowship from the National Elite Foundation of Iran. He was also the recipient of the Atwood Fellowship in the fall of 2010 and the 2014 Intel/Texas Instruments/Catalyst Foundation CICC Student Scholarship Award.

Azita Emami-Neyestanak (S'97–M'04) was born in Naein, Iran. She received the B.S. degree (with honors_ from Sharif University of Technology, Tehran, Iran, in 1996, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1999 and 2004, respectively.

She is currently a Professor of Electrical Engineering with the California Institute of Technology, Pasadena, CA, USA. From July 2006 to August 2007, she was with Columbia University, New York, NY, as an Assistant Professor with the Department of Electrical Engineering. She was also a Research Staff Member with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, from 2004 to 2006. Her current research areas are high-performance mixed-signal integrated circuits and VLSI systems, with the focus on high-speed and low-power optical and electrical interconnects, clocking, biomedical implant, and compressed sensing.