This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

A 25Gb/s 3D-Integrated CMOS/Silicon-Photonic Receiver for Low-Power High-Sensitivity Optical Communication

Saman Saeedi, *Student Member, IEEE*, Sylvie Menezo, *Member, IEEE*, Gabriel Pares, *Member, IEEE*, and Azita Emami, *Member, IEEE*

***Abstract*— Integrating optical receivers based on double-sampling architecture exhibit a low-power alternative to those designed around transimpedance amplifiers (TIA). In this paper, we present a 3D-integrated CMOS/Silicon photonic optical receiver. The receiver features a low-bandwidth TIA integrating front-end, double-sampling technique and dynamic offset modulation. The copper-pillar based 3D-integration technology used here enables ultra-low parasitics and 40µm pitch for interconnection. We study different trade-offs in designing an optical receiver and how to choose between a full-bandwidth TIA front-end and integrating architecture using a resistive front-end or a low-bandwidth TIA front-end. The design methodology is supported by measurements of two 3D-integrated prototypes based on a conventional TIA and a double-sampling integrating receiver. The proposed receiver architecture achieves -14.9dBm of sensitivity and energy efficiency of 170fJ/b at 25Gb/s while the conventional receiver achieves a sensitivity of –10.4dBm and energy efficiency of 260fJ/b at 21.2Gb/s.**

***Index Terms*—Optical receivers, energy efficiency, sensitivity, silicon photonics, 3D integration.**

I. Introduction

Optical interconnects are promising candidates to overcome deficiencies of electrical channels. As silicon photonic and integration technologies are maturing, commercialization of these technologies is becoming closer to reality. High-density, low-parasitic heterogeneous integration technologies are essential elements in implementation of high-speed, high-sensitivity optical links. Advancement in heterogeneous integration technologies has been focused on higher density and lower capacitive, resistive and inductive parasitics. The motivation behind this trend is that the extra capacitor due to bonding added to photo-detector's (PD) capacitor creates the dominant pole (ω_{p1}) of the TIA (Fig. 1).

Manuscript received on July 22, 2015; revised September 25, 2015; accepted October 15, 2015.

S. Saeedi and A. Emami are with California Institute of Technology, 1200 E California Blvd., Pasadena, CA 91125, USA (e-mail: saman.saeedi@caltech.edu; azita@caltech.edu).

S. Menezo and G. Pares are with CEA-Leti, Minatec-Campus, DOPT, 17 Rue des Martyrs, 38054 Grenoble Cedex 9, France (e-mail: sylvie.menezo@cea.fr; gabriel.pares@cea.fr).

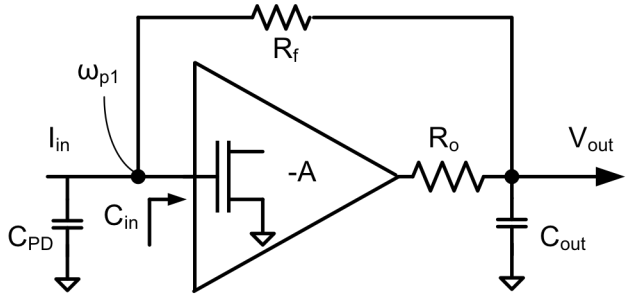


Fig. 1. A resistive feedback TIA model.

This is the limiting factor in speed of conventional optical receivers based on TIAs. Also, in parallel optical receivers bond-wire can be a source of crosstalk between channels.

For a given integration technology, the input impedance of the TIA has to be reduced to push the dominant pole further. This is achieved by higher amplifier gain. However, higher gain comes at the cost of increased power consumption or by increasing the gain-bandwidth by area-consuming techniques such as inductive peaking. Integrating receivers have been introduced aiming at removing these limitations [1]. In an integrating optical receiver based on double-sampling, the photocurrent is integrated on the front-end capacitor and is sampled at the beginning and end of the bit-time interval. A comparator, e.g. a strongARM sense amplifier, is used to distinguish ones and zeros by determining which sample is

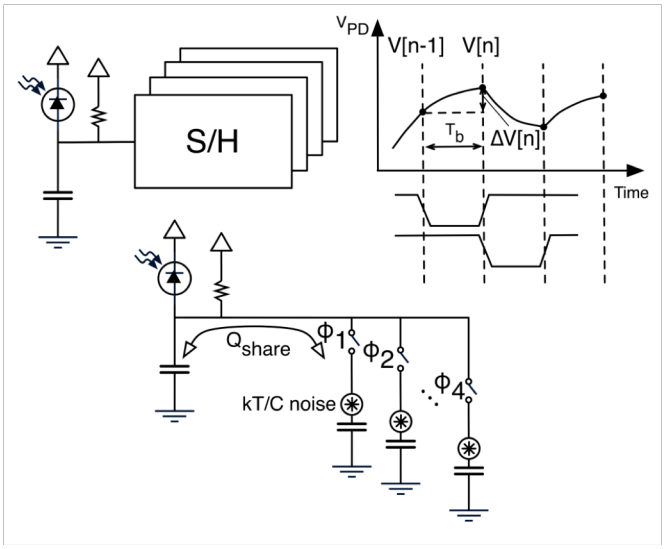


Fig. 2. In double sampling receivers with resistive front-end sensitivity is limited by charge sharing and kT/C noise.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

larger. Due to integrating nature of the optical receiver the pole associated with this front-end cap is not the bottleneck for achieving higher data-rates. In integrating front-ends with a resistive termination, the charge integrated on the front-end capacitor gets shared with sampling capacitors (Fig. 2) causing sensitivity degradation. This issue has been addressed by adding a low-bandwidth TIA to the front-end in this work [2], [3]. The low-bandwidth TIA provides isolation between PD's capacitor and sampling capacitors, which reduces charge-sharing effect and enables use of ultra-low capacitance PDs in advanced silicon photonic technologies.

In this paper, we aim at developing a design guideline to choose between low-bandwidth TIA, resistive and full-bandwidth TIA front-ends. In order to evaluate different receiver designs and target a specific performance, various parameters can be considered. Power consumption, energy efficiency, sensitivity and operational data-rate with a specific bit error-rate (BER) are some of these parameters. However, there are inherent trade-offs between these parameters and they cannot be independently enhanced. The question is how to assess performance of different designs and decide which one is superior. Different figure of merits (FoM) have been proposed to quantify overall performance of optical receivers and compare them. For example, [4] uses

$$FoM_{Sensitivity} = \frac{Sensitivity\ (Watts_{pp}) \times Responsivity_{PD}}{C_{in} \times Data\ Rate} \quad (1)$$

to quantify design performance based on receiver's sensitivity. In many other cases such as [5], the following FoM is used:

$$FoM_{TIA} = \frac{Gain \times Bandwidth}{Power} \quad (2)$$

From an optical link system perspective, one of the most important metrics is the total power consumption, which includes the power of laser at the transmitter side [6]. From receiver circuit design perspective, the two main factors that determine the overall power consumption are sensitivity and electrical power consumption. Equation (3) defines an FoM to capture the impact of receiver on total power consumption of the optical link due to both electrical and optical components.

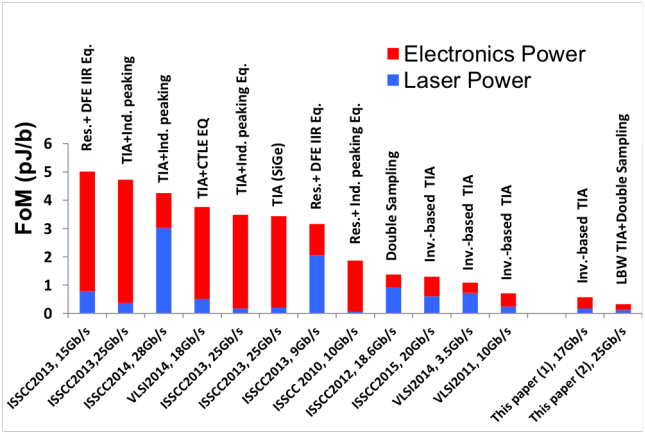


Fig. 3. Recently published optical receivers.

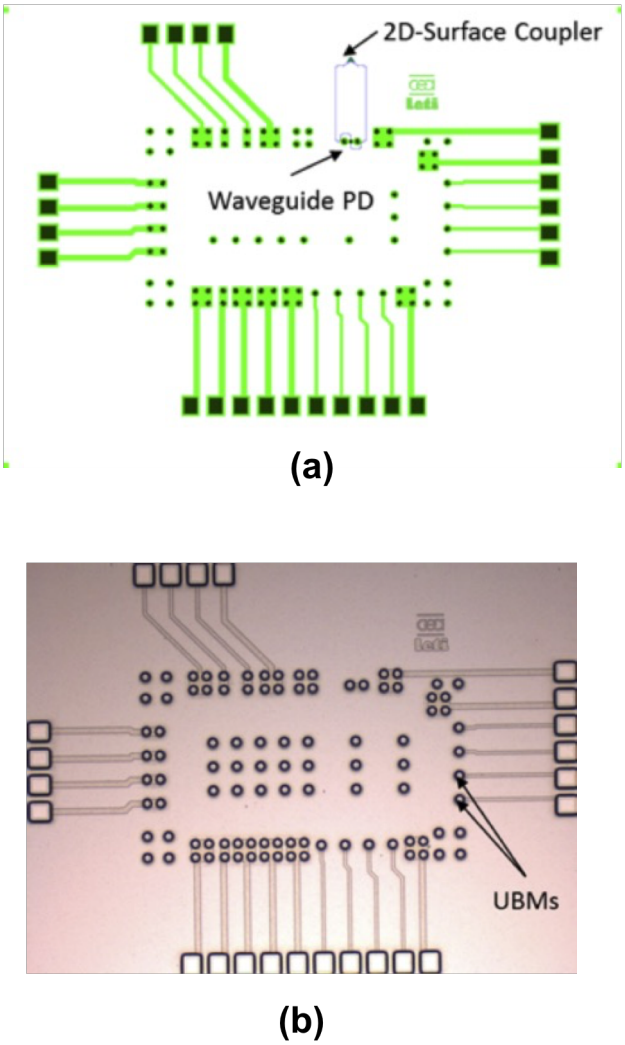


Fig. 4. (a) Layout of the silicon photonic chip. (b) Die micrograph of the fabricated silicon photonic chip.

$$FoM_{power} = \frac{Power_{electrical} + K \times Sensitivity(Current_{pp})}{Data\ Rate} \quad (3)$$

Where K captures the laser efficiency, optical coupling losses and responsivity of the photodiode (4).

$$K = \frac{Efficiency_{laser} \times Coupling\ losses}{Responsivity_{PD}} \quad (4)$$

Note that while the electrical power of transmitter circuitry is not included in (2), the laser power, modulator's insertion loss and its coupling losses are taken into account. This is because the receiver sensitivity determines the laser power and the coupling losses are proportional to initial laser power. It is instructive to plot (3) for some recently reported optical receivers based on different receiver architectures [2]-[15] (Fig. 3). The portion of power consumption associated with laser (blue) and electronics (red) is separated. K is calculated for a responsivity of 0.8A/W, laser wall-plug efficiency of 15%, and coupling loss of 3dB for a transmitter architecture

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

based on CW laser and MZI-based modulator. As can be seen, the laser power is important and often the dominating factor.

Advancement in integrated photonics, CMOS scaling and packaging technology such as the 3D-integrated optical receiver presented in [16] help reducing the overall power consumption of an optical link. However, the choice of circuit topology and its sensitivity can play an important role in optimal overall link design and reduction of total power consumption. In light of the discussion above, we present a compact 3D integrated optical receiver, which is designed specifically to take advantage of advanced silicon-photonics and low-parasitic integration technology to achieve high sensitivity and low power consumption. The low-bandwidth TIA front-end enhances sensitivity of the double-sampling receiver architecture and enables realization of a high-sensitivity optical receiver operating at 25Gb/s.

This paper is organized as follows. Section II briefly introduces the 3D integration technology based on Copper Pillar (CuP) bonding. Section III explains the overall architecture of the optical receiver. Section IV provides analysis and a design guideline to determine which front-end is suitable depending on available technology and system requirements. Section V provides measurements results. Finally, section VI is the summary and conclusion of the paper.

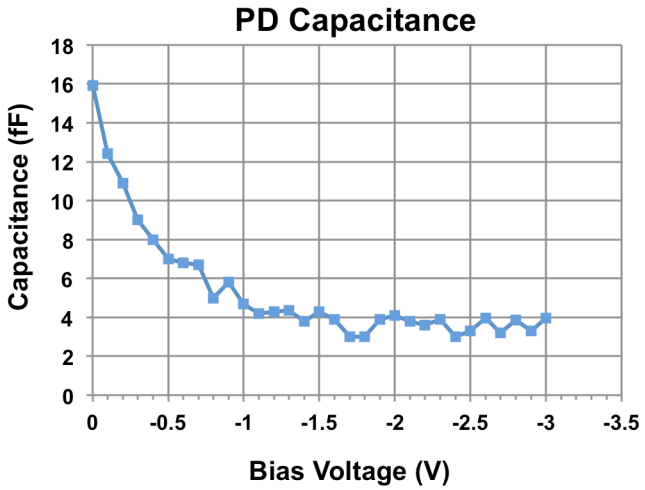


Fig. 5. Measured photo-detector capacitance as a function of bias voltage.

II. CMOS/Silicon Photonic 3D-Integrated Platform

The silicon photonic chip in this receiver is designed in Leti's advanced silicon photonic platform and comprises of a 2D surface grating coupler, which has two outputs coupled to a waveguide photo-detector. This technology enables low parasitic capacitance and dense interconnections of CMOS and Silicon Photonics. Fig. 4 shows the layout and die micrograph of the silicon photonic chip. The chip is designed such that electrical connections to CMOS chip are routed through silicon photonic die. Fig. 5 shows PD capacitance as a function of reverse bias voltage. For a reverse bias of -0.5V to -2V, the PD capacitance is measured to be less than 8fF. The -3dB bandwidth of the PD is measured to be larger than 18GHz when terminated with a 50Ω resistor.

The 3D-integration involves Under Bump Metallization (UBM) of the silicon photonic chip, and growth of copper micro-pillars on the Electronic wafer. The EIC was then flip-chip mounted on the Si-PIC. Fig. 4 (b) shows the die micrograph of the Silicon photonic chip with UBM processed on the photonic wafer. Fig. 6 (a) shows the scanning electron microscope (SEM) top view of the CuP grown on the electronic wafer and Fig. 6 (b) shows the cross section of the

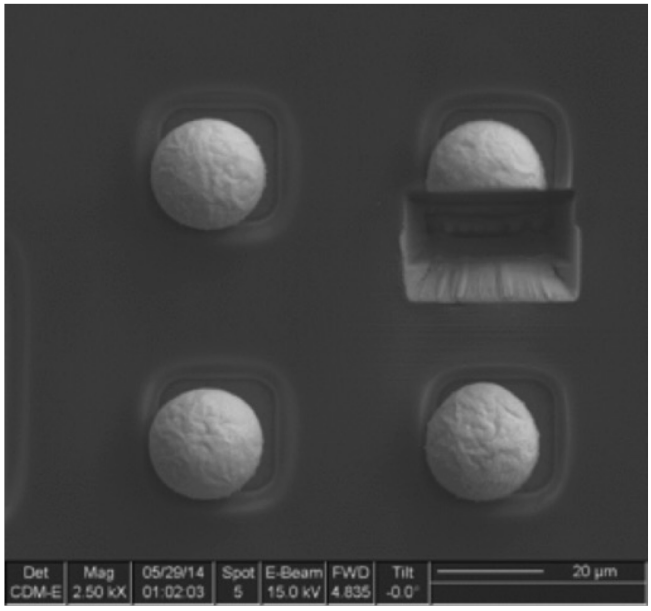


Fig. 6. (a) Scanning electron microscope top view of the CuP grown on the electronic wafer. (b) cross section of the micro-pillar.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

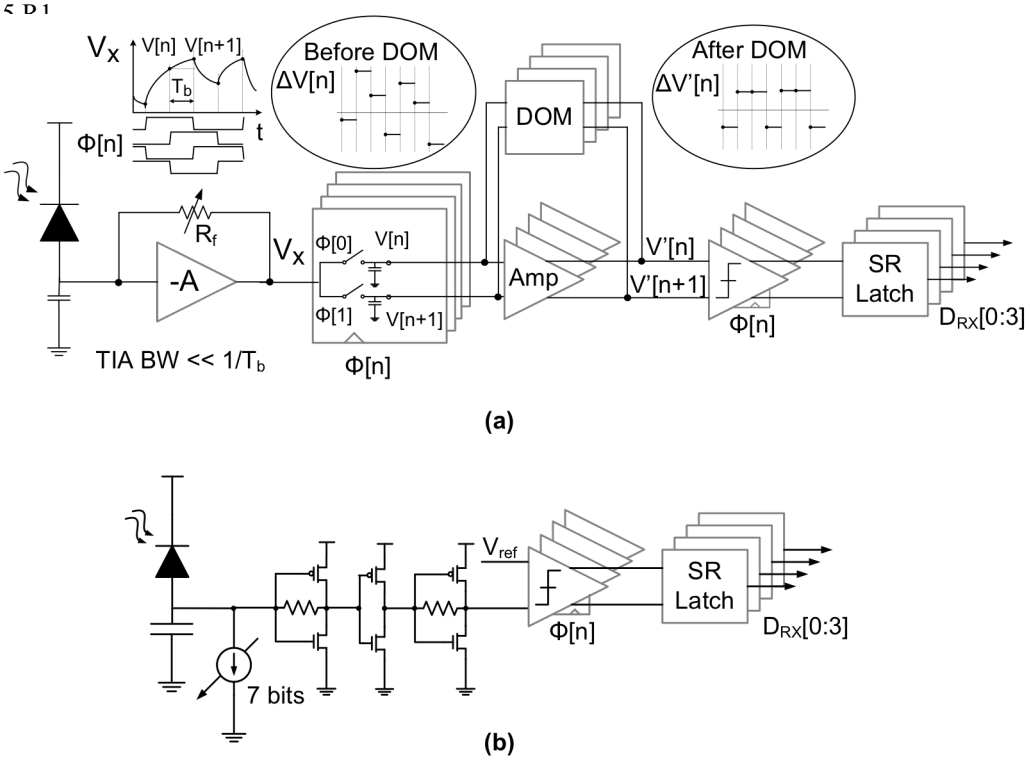


Fig. 7. Top-level architecture of (a) integrating receiver with low-bandwidth TIA (b) TIA-based receiver.

micro-pillar. The minimum pitch for adjacent copper pillar bonds is 40μm, allowing realization of dense optical links [17]. The parasitic capacitance and resistance associated with each bonding is measured to be less than 25fF and 1Ω. The parasitic inductance is negligible. This low-parasitic integration is one of the key elements for achieving high bandwidth and high sensitivity optical links.

III. Receiver Architecture

Fig. 7 shows the proposed integrating receiver and a conventional TIA-based receiver designed for comparison. In conventional receivers, TIAs are used to reduce the input impedance and increase the bandwidth. In this work a scalable 3-stage TIA, based on inverters with a resistive feedback, is used. This architecture is particularly suitable for highly scaled CMOS technologies and consumes relatively low power and area. The proposed integrating receiver uses a low-power, low-bandwidth TIA as front-end with a bandwidth that is much lower than the bit-time interval. Note that the integrating nature of the receiver comes from the sampling node (output of the low-bandwidth TIA). At this node, the impedance of the sampling capacitors at frequency of operation is much lower than the output impedance of the low-bandwith TIA. Therefore, most of the charge is integrated on the sampling capacitors. The low bandwidth TIA's output is sampled at the beginning and end of the bit time (T_b). These samples, (V[n], V[n+1]) are then compared to resolve each bit ($\Delta V[n] < 0$

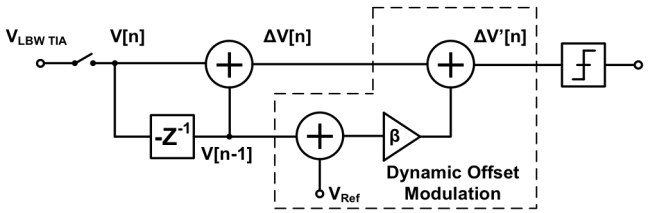


Fig. 8. Z-domain block diagram of the integrating optical receiver with low-bandwidth TIA.

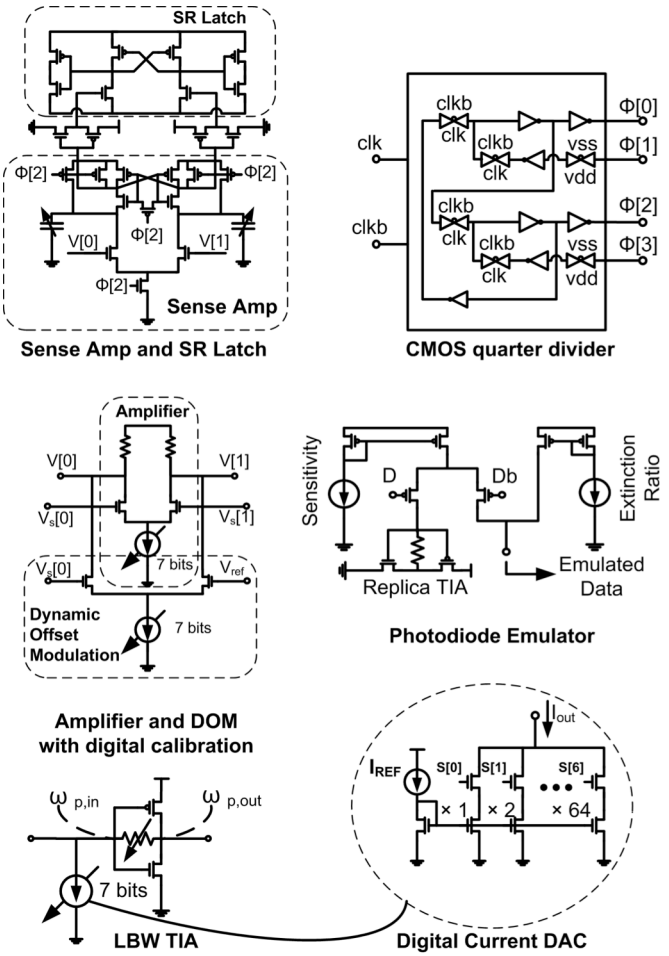


Fig. 9. Circuit-level implementation of individual building blocks.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

results in "1" and ΔV[n] > 0 results in "0"). Note that the voltage difference, ΔV[n], is input pattern dependent due to low-bandwidth nature of the front-end. For example a "1" followed by a long sequence of "0" generates a stronger ΔV[n] compared to a "1" followed by many "1"s.

Dynamic offset modulation (DOM) is utilized to provide a constant voltage at sense-amp's input irrespective of the stream of data [18]. DOM essentially increases the voltage difference for weak ones/zeros and decreases it for strong ones/zeros. The underlying principle used for DOM is that identical consecutive bits shift the sampling node voltage away from its DC average. So, the introduced offset is proportional to the value of the voltage at the sampling node compared with its DC average. The DOM will be investigated using z-domain analysis later in this section.

Double sampling technique allows de-multiplexing by using multiple clock phases and samplers. The poles associated with input and output nodes of the LBW TIA are as follows

$$\omega_{p,in} = \frac{1+A}{R_f(C_{in}+C_{PD})}. \quad (5)$$

$$\omega_{p,out} = \frac{1}{4R_fC_{S/H}}. \quad (6)$$

Where R_f is the feedback resistance, C_{in} is the capacitance looking into the TIA and C_{PD} is the photodiode and parasitic capacitance combined. Fig. 8 shows the simple model for the receiver in z-domain. The voltage of the sampler can be written in z-domain as

$$V(z) = \left(\frac{R_fI_{pd}}{1+\frac{1}{A}}\right)\left[\frac{1}{1-e^{-\frac{T_b}{\tau_{p1}}}z^{-1}} + \frac{1}{1-e^{-\frac{T_b}{\tau_{p2}}}z^{-1}}\right]. \quad (7)$$

Where T_b is the bit time interval and τ_{p1} and τ_{p2} are time constants associated with low-bandwidth TIA poles. By subtracting the previous sample, V[n-1], from V[n] the result, ΔV, can be written in z-domain as

$$\Delta V'(z) = V(z)(1-z^{-1}) - \beta z^{-1}V(z). \quad (8)$$

Where β is the DOM coefficient and has to be chosen such that $\Delta V'$ becomes independent of z. β can be found only if the low-bandwidth TIA is designed with its output pole at much lower frequency compared to $1/T_b$ and the input node is at a higher frequency compared to $1/T_b$. In that case by choosing β as

$$\beta = 1 - T_b/\tau_{p1} \quad (9)$$

the DOM provides a constant voltage at sense-amp's input regardless of the data sequence. This constant voltage is given by (10).

$$\Delta V' \approx \frac{R_fI_{pd}\left(1-e^{-T_b/\tau_{p1}}\right)}{2(1+1/A)} \quad (10)$$

Fig. 9 shows details of circuit level implementation for the optical receiver's building blocks. The high-speed sense-amp has digital offset cancellation using a bank of 5 NMOS capacitors in accumulation mode. The sense-amp is followed by an SR-latch to retrieve the NRZ data. A CMOS quadrature divider is used to generate the four phases required for operation of the optical receiver. Sampling capacitors are followed by an amplifier with a gain of 4.5dB, which also provides isolation between sampling nodes and sense-amp to minimize kickback. Dynamic offset modulation that is employed at the output of the amplifier is also implemented as another differential pair, sharing the same load. The photodiode emulator is a high-speed open-drain PMOS pair that steers a pre-set current between replica low-bandwidth TIA and the optical receiver under test. A separate current mirror is used to set the extinction ratio. The low-bandwidth TIA has a transimpedance of 3kΩ and has a digitally controlled 7-bit current DAC at its input to set the DC point at the input of the low-bandwidth TIA. The S/H capacitor is chosen to be 12fF to minimize noise and current sensitivity while achieve 25Gb/s operational data-rate.

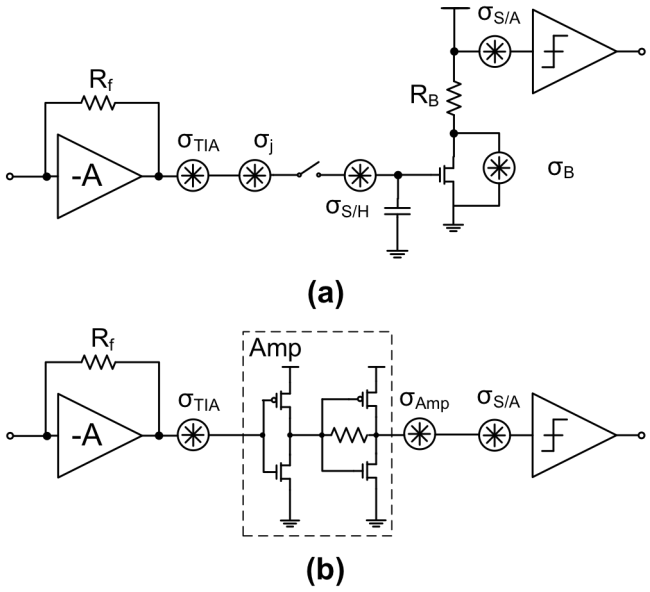


Fig. 10. Noise sources for (a) integrating optical receiver and (b) conventional TIA-based optical receiver.

IV. Analysis and Design Guideline

Input referred noise is the critical parameter determining the sensitivity of an optical receiver. Multiplying it by the signal to noise ratio (SNR), which is calculated for a target BER, yields receiver's current sensitivity. The gain of the TIA's first stage has a critical role as noise of all subsequent stages gets divided by this gain. When designing an inverter-based TIA, for a given CMOS technology, there is a maximum gain-bandwidth product a single stage can achieve. Thus, the gain has to be reduced to achieve sufficient bandwidth at high data-rates. Lower gain at the first stage worsens the sensitivity of the receiver. Fig. 10 shows noise sources for integrating receiver and the conventional TIA-based receiver. The minimum required current for the integrating receiver operation is

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

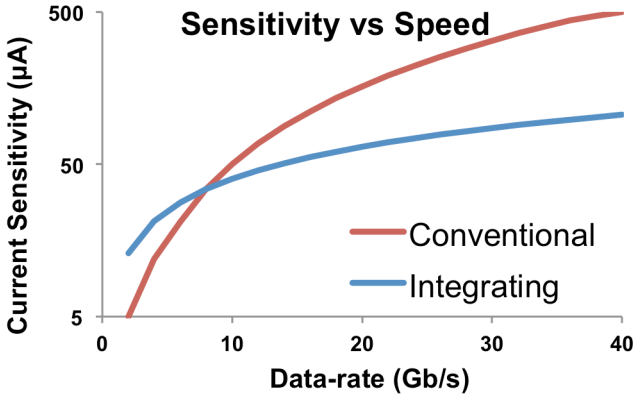


Fig. 11. Simulated sensitivity vs. speed for integrating and conventional optical receivers.

$$\boldsymbol{I_{b,integrating}} = SNR \times \sigma_{n,prop.} + \frac{1}{R_{LBW,TIA}} \times \frac{V_{offset}}{A_B} \quad (11)$$

where $\sigma_{n,prop}$ is the total input referred noise for the integrating receiver, V_{offset} is the residual sense-amp offset after calibration, A_B is the buffer gain and $R_{LBW,TIA}$ is the low-bandwidth TIA's transimpedance. In the case of conventional TIA-based receiver, we have

$$\boldsymbol{I_{b,conventional}} = SNR \times \sigma_{n,conv.} + \frac{1}{R_{TIA}} \times \frac{V_{offset}}{A_{AMP}} \quad (12)$$

where $\sigma_{n,conv}$ is the total input referred noise for the conventional receiver, A_{AMP} is the amplifier gain and R_{TIA} is the TIA transimpedance.

Referring all noise sources to input, the total input referred noise can be written as

$$\overline{\boldsymbol{\sigma^2_{n,prop}}} = \frac{1}{R^2_{LBW,TIA}} \left(\overline{\sigma^2_{S/H}} + \overline{\sigma^2_B} + \frac{\overline{\sigma^2_{SA}}}{A^2} + \overline{\sigma^2_J} + \overline{\sigma^2_{LBW\,TIA}} \right). \quad (13)$$

Similarly, the input referred noise of the conventional TIA-based receiver could be written as

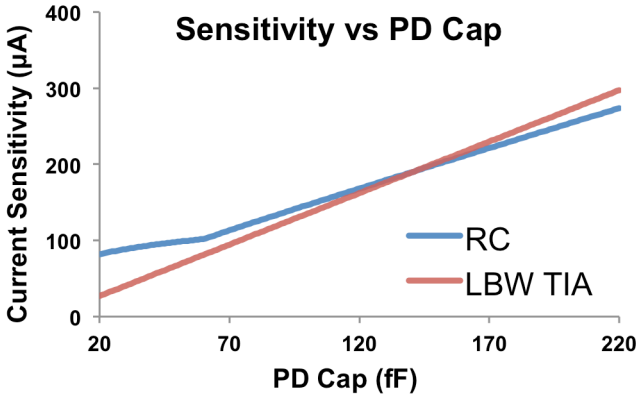
$$\overline{\boldsymbol{\sigma^2_{n,conv}}} = \frac{1}{R^2_{TIA}} \times \left(\frac{\overline{\sigma^2_{AMP}} + \overline{\sigma^2_{SA}}}{A^2} + \overline{\sigma^2_{TIA}} \right). \quad (14)$$

For a given power consumption, the gain-bandwidth product of the TIA stage is constant. Therefore, by choosing larger $R_{LBW,TIA}$ compared with R_{TIA} the overall sensitivity improves.

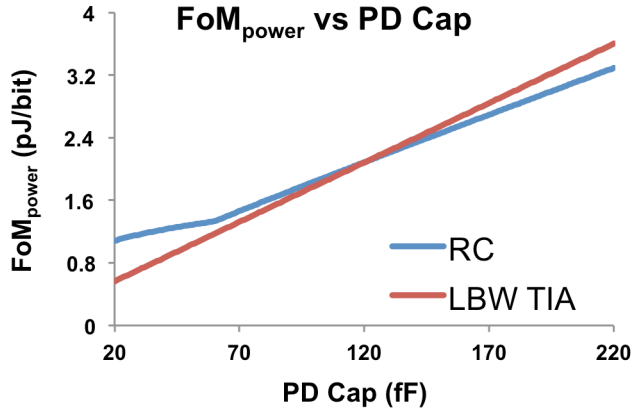
The sense-amp noise contribution could be modeled as a sampler with gain, which has an input referred noise of [17]

$$\overline{\boldsymbol{\sigma^2_{SA}}} = \frac{1}{R^2_{TIA}} \times \frac{2kT}{A^2_{SA} C_A} \quad (15)$$

where C_A is the sense-amp decision node capacitance, A_{SA} is the sense-amp gain. This capacitance is set to be about 15fF to cover the expected offset range. The sense-amp has a gain close 1.1 which results in a sense-amp input referred noise of about $(0.2\mu A)_{rms}$. The buffer noise is calculated as



(a)



(b)

Fig. 12. (a) Simulated sensitivity vs. PD capacitor for RC and low-bandwidth TIA front-end at 25Gb/s (b) FoM vs. PD capacitor for RC and low-bandwidth TIA front-end at 25Gb/s.

$$\overline{\boldsymbol{\sigma^2_B}} = \frac{1}{R^2_{TIA}} \times \frac{8kT}{g_m} \left(\gamma + \frac{1}{R_B} \right) \quad (16)$$

where γ is the transistor noise coefficient, g_m is the transconductance of the stage and R_B is the load resistance. This noise contribution of this buffer stage with 4.5dB of gain is simulated to be around $(0.22\mu A)_{rms}$. The sampling capacitor's noise contribution is equal to

$$\overline{\boldsymbol{\sigma^2_{S/H}}} = \frac{1}{R^2_{TIA}} \times \frac{2kT}{C_{S/H}}. \quad (17)$$

The factor of two is due to the fact that we have two differential sampling capacitors connected to the buffer. Clock jitter is also an important factor when calculating the receiver sensitivity. Deviations from ideal sampling time translate to voltage level uncertainties in the sampling voltages that could be modeled as a noise source with variance of

$$\overline{\boldsymbol{\sigma^2_J}} = \frac{1}{R^2_{TIA}} \times \left(\frac{\sigma_{CLK}}{T_b} \right)^2 \Delta V_b^2 \quad (18)$$

where σ_{CLK} is the clock RMS jitter [18]. Given the measured clock RMS jitter of 0.9ps, σ_J is calculated to be around

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

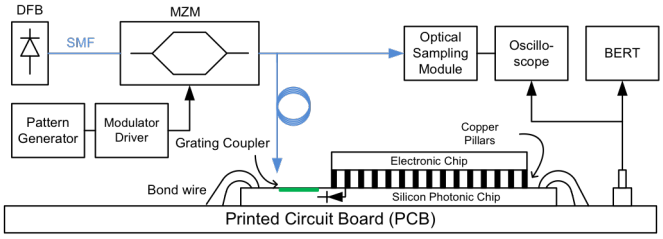


Fig. 13. Optical measurement setup.

$(0.17\mu A)_{rms}$. The total noise due to dynamic offset modulation is measured to be

$$\overline{\sigma_{DOM}^2} = \frac{1}{R_{TIA}^2} \times \frac{\beta^2}{2A^2}\left(\overline{\sigma_J^2} + \overline{\sigma_S^2} + 2\overline{\sigma_B^2}\right). \quad (19)$$

This contribution is negligible as the dynamic offset modulation coefficient, β, is much smaller than buffer gain, A. Finally, the low-bandwidth TIA noise is simulated to be $(0.18\mu A)_{rms}$.

It is instructive to plot I_b as a function of operational data-rate. To do so, the required bandwidth in GHz is set to be 0.7 times data-rate in GHz and the gain and bandwidth is simulated for each data-rate for the given technology, 28nm bulk CMOS. The resulting sensitivity vs. data-rate trade-off is shown in Fig. 11. Note that the crossing point where conventional TIA-based receiver achieves better sensitivity is 8Gb/s. Above this data-rate, the gain of the TIA stage has to be reduced to achieve the required bandwidth and (18) becomes larger than (19). At low data-rates, the additional terms present in (18) make the current sensitivity of the integrating receiver larger.

Another design consideration in integrating receivers is the choice between resistive and low-bandwidth front-ends. To investigate this, we simulated sensitivity of RC and low-bandwidth TIA front-ends at 25Gb/s using different PD capacitances. A ratio of × 10 ratio between the photo-detector capacitor and the sampling capacitor is assumed to avoid excessive charge sharing. The minimum controllable capacitance for sample-and-hold is around 3.5fF, limited by next stages parasitic capacitance. Fig. 12(a) shows simulation of sensitivity vs. photodiode capacitance. As can be seen, for a PD capacitance below 135fF, the low-bandwidth TIA front-end achieves better sensitivity. Note that this is true even for a different data-rate as in both LBW TIA and RC front-end cases the sensitivity is dominated by integration time and linearly increases with data-rate. In order to account the power overhead consumed by the low-bandwidth TIA, the FoM defined in (3) is plotted for a data-rate of 25Gb/s in Fig. 12 (b). In this case, the low-bandwidth TIA front-end becomes superior for a PD capacitance below 115fF. If we run this simulation for higher data-rates TIA front-end becomes superior for a higher PD capacitance. That is because the power consumption of digital elements and sensitivity linearly scales with data-rate but the power consumption of LBW TIA remains relatively unchanged.

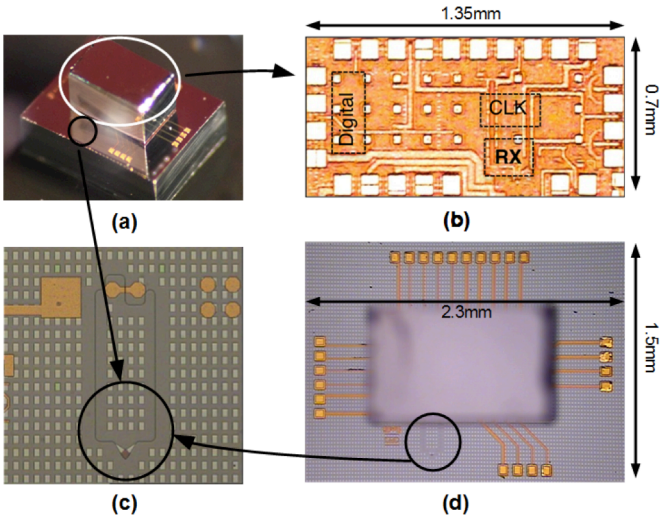


Fig. 14. (a) 3D-integrated CMOS/silicon-photonic optical receiver (b) CMOS chip die micrograph (c) Grating coupler and polarization splitter on the silicon photonic chip (d) Top-view of the 3D-integrated optical receiver.

V. Measurement Results

Fig 13 shows the optical measurement setup used for testing the chips. Two prototypes are fabricated in a 28nm CMOS technology to compare performance of the integrating architecture with a conventional TIA-based receiver. Receivers occupy an active area of $0.0018mm^2$. The 3-stage TIA architecture design is optimized to have maximum bandwidth for the given technology (28nm CMOS). Fig. 14(a)-(d) show the 3D integration of electronics/photonics as well as the top view of CMOS and SiPh chips. Each prototype is comprised of two receivers, one with a photodiode emulator (Fig. 9) and one for optical testing with 3D-integrated silicon photonics. Initial verifications were done using the on-chip emulator, which mimics the photodiode current with an on-chip switchable current source and a bank of capacitors, to emulate the parasitic capacitances due to PD and bonding. An on-chip CML-to-CMOS converter generates the full swing clocks from an off-chip clock source and the four phases of clock are generated using an on-chip quadrature divider. The

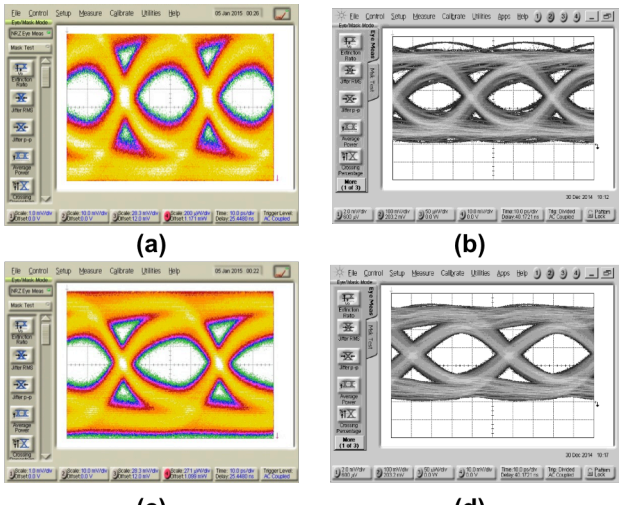


Fig. 15. (a) Input optical eye diagram at 25Gb/s for integrating receiver (b) Output recovered and de-multiplexed eye diagram at 6.25Gb/s for the integrating receiver (c) Input optical eye diagram at 21.2Gb/s for the conventional receiver (d) Output recovered and de-multiplexed eye diagram at 6.25Gb/s for the conventional receiver.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

on chip clock was measured to have about 8-ps peak-to-peak jitter.

The functionality of the receiver was first validated using the on-chip emulator and PRBS7, PRBS9, PRBS15 sequences. R and C_{in} were chosen 3kΩ and 50fF ($4R_fC_{SH} \approx 150$ps). Functionality of the DOM for long sequences of ones or zeros was validated using a 100 MHz square-wave current applied to the input to the receiver while the front-end sampled the input at 25 Gb/s. In this case, 250 consecutive zeros will be followed by 250 ones. For an input time constant of about 0.105ns, these 250 consecutive bits push the input to the saturation limits.

Fig. 15 shows the optical input eye diagram and output recovered and de-multiplexed eye diagram for both receivers at their maximum speed. The silicon photonic chip uses a grating coupler to couple light from an off-chip source. The

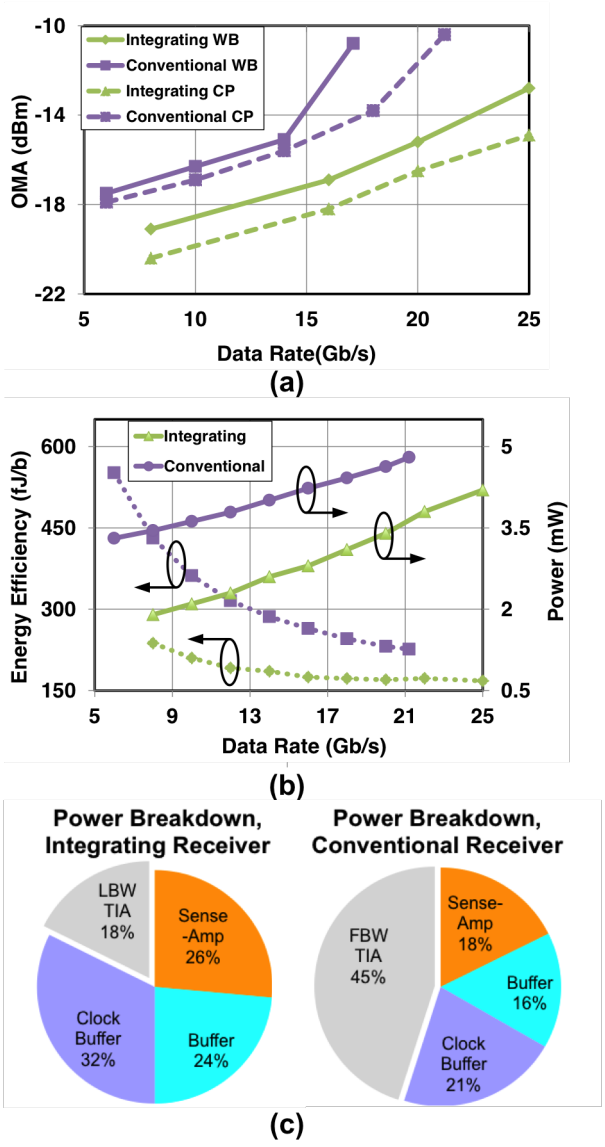


Fig. 16. Optical measurement results (a) Sensitivity of integrating and conventional receivers bonded with CuP and wire-bond (b) Energy efficiency and power consumption of the optical receiver (c) Power consumption breakdown for integrating and conventional receiver.

capacitance due to the CuP bonds and pad is estimated to be

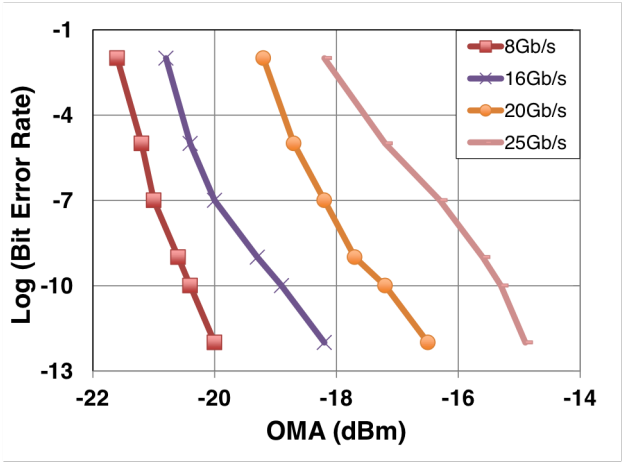


Fig. 17. Sensitivity curves of the integrating optical receiver.

less than 25fF and the photodiode capacitance is measured to be less than 8fF. The optical beam from a 1550nm DFB laser diode is modulated by a high-speed Mach-Zehnder modulator and coupled to the photodiode through a single-mode fiber. The PD responsivity including grating coupler losses was measured to be 0.2A/W.

The receivers were tested using PRBS-15 sequence. The maximum achievable data-rates for the integrating receiver and conventional receiver are measured to be 25Gb/s and 21.2Gb/s respectively. Fig. 16(a) shows measured sensitivity vs. data-rate for both receivers, bonded with wire-bond and CuP integration. For bit-error rate (BER) of 10^{-12}, the conventional receiver requires -10.4dBm of optical modulated amplitude (OMA) at 21.2Gb/s (its maximum speed), while the integrating architecture requires OMA of -16.1dBm at 21.2Gb/s and -14.9dBm at 25Gb/s. The coupling loss,

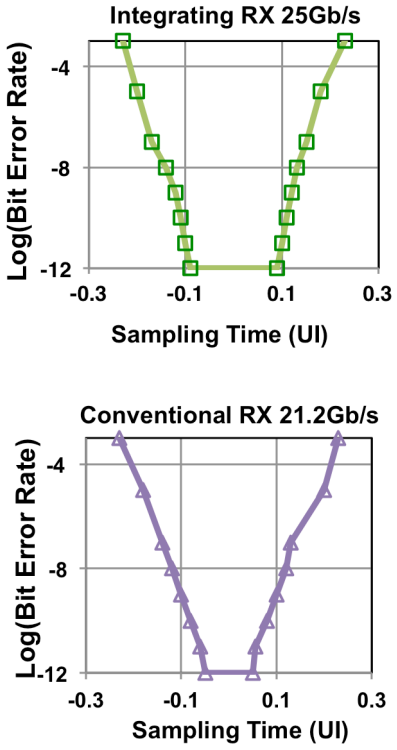


Fig. 18. Measured bathtub curves of the integrating receiver and conventional TIA-based receiver.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JLT.2015.2494060, Journal of Lightwave Technology

measured to be 6dB is included in these measurements. Fig. 16 (b) shows power consumption and energy efficiency of the receivers at different data rates. In both designs, the power of digital elements increases linearly with speed. The 3-stage TIA design offers per-bit energy consumption of 226fJ/b at 21.2Gb/s compared with the integrating architecture that has per-bit energy consumption of 171fJ/b at 21.2Gb/s. Energy efficiency of the integrating design reaches its peak of 170fJ/b at 25Gb/s. Fig. 16 (c) shows power consumption break-down for both receivers. Fig. 17 shows the sensitivity curves of the integrating optical receiver at different data-rates. The coupling loss (measured to be 6dB) is included in this plot.

Fig. 18 shows bathtub curves of receiver designs at their respective maximum operational speeds. Table 1 summarizes the performance of the designed optical receivers and compares them to the state-of-the-art.

VI. Conclusion

The double-sampling receiver with dynamic offset modulation and low-bandwidth TIA is well suitable for 3D integration and advanced silicon photonic technologies. Experimental results validated the feasibility of an ultra-low power 25Gb/s receiver and its superior performance over a conventional TIA-based architecture in terms of power consumption, sensitivity and speed. It was shown that for the proposed architectures, the integrating receiver with a low-bandwidth TIA achieves higher sensitivity at data-rates higher than 8Gb/s compared with conventional TIA-based receiver. Also, we demonstrated that when the front-end input capacitance is smaller than 135fF, higher sensitivity is achieved by employing a low-bandwidth TIA instead of simple resistive front-end. So, for the presented particular topologies the target data-rate determines the choice between conventional and integrating receivers. If an integrating receiver is chosen, the input node capacitance determines the choice between a LBW TIA front-end and a resistive front-end. Two prototypes were fabricated and fully tested to validate our analysis. The double-sampling optical receiver with low-bandwidth TIA and dynamic offset modulation consumes 170µW/Gb/s while operating at 25Gb/s. It has an optical sensitivity of -16.1dBm at 21.2Gb/s, which drops to -14.9dBm at 25Gb/s. The conventional TIA-based receiver consumes 226µW/Gb/s while operating at 21.2Gb/s and has an optical sensitivity of -10.4dBm.

TABLE I
Performance Summary and Comparison

		Int. Arch.	Conv. Arch.	[7]	[8]	[18]	[19]
Technology		28nm	28nm	40nm	65nm	65nm	90nm
Data Rate (Gb/s)		25	21.2	10	28	24	16
Efficiency (mW/Gb/s)		0.17	0.26	0.395	3.25	0.4	1.4
Area (mm^2)		0.0018	0.0018	-	0.32	0.0028	0.025
RX C_{in} (fF)		<25	<25	60	-	<200	440
Sensitivity	Current (µA)	25 @ 25Gb/s	71 @ 21.2Gb/s	-	86 @ 25Gb/s	160 @ 24Gb/s	284 @ 16Gb/s
	Optical (dBm)	-14.9* @ 25Gb/s	-10.4* @ 21.2Gb/s	-15*** @ 10Gb/s	-9.7 @ 25Gb/s	-4.7** @ 24Gb/s	-5.4** @ 16Gb/s

* Optical measurement at photodiode.
** Optical measurements, coupling losses are not considered.
*** Estimated through current sensitivity, knowing responsivity of the PD.

Acknowledgment

The authors would like to thank ST Microelectronics for chip fabrication.

References

[1] A. Emami-Neyestanak, D. Liu, G. Keeler, N. Helman, and M. Horowitz, "A 1.6 Gb/s, 3 mW CMOS receiver for optical communication" in *IEEE Symp. VLSI Circuits Dig. Of Tech. Papers*, 2002, pp. 84-87.

[2] S. Saeedi, S. Menezo, and A. Emami, "A 25Gbps 3D-integrated CMOS/silicon photonic optical receiver with -15dBm sensitivity and 0.17 pJ/bit energy efficiency," in *IEEE Optical Interconnects Conf. (OI)*, 2015, pp. 11-12.

[3] S. Saeedi, and A. Emami, "A 25Gb/s 170µW/Gb/s optical receiver in 28nm CMOS for chip-to-chip optical communication," in *IEEE Radio Freq. Int. Circuits Symp.*, 2014, pp. 283-286.

[4] J. Proesel, A. Rylyakov, and C. Schow, "Optical receivers using DFE-IIR equalization," in *IEEE Intl. Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC)*, 2013, pp. 130-131.

[5] G. Kalogerakis, T. Moran, T. Nguyen, and G. Denoyer, "A quad 25Gb/s 270mW TIA in 0.13µm BiCMOS with< 0.15 dB crosstalk penalty," in *IEEE Intl. Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC)*, 2013, pp. 116-117.

[6] I. Young, E. Mohammed, J. T. Liao, A. M. Kern, S. Palermo, B. Block, M. R. Reshotko, and P. L. Chang, "Optical I/O technology for tera-scale computing," *IEEE J. Solid-State Circuits*, Vol. 45, no. 1, pp. 235-248, Jan. 2010.

[7] F. Liu , D. Patil, J. Lexau, P. Amberg, M. Dayringer, J. Gainsley, H. Fathi Moghadam et al., "10 Gbps, 530 fJ/b optical transceiver circuits in 40 nm CMOS," in *IEEE Symp. VLSI Circuits Dig. Of Tech. Papers*, pp. 290-291, 2011.

[8] T. Takemoto, H. Yamashita, T. Yazaki, N. Chujo, Y. Lee, and Y. Matsuoka, "A 4× 25-to-28Gb/s 4.9 mW/Gb/s− 9.7 dBm high-sensitivity optical receiver based on 65nm CMOS for board-to-board interconnects," in *IEEE Intl. Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC)*, pp. 118-119, 2013.

[9] M. H. Nazari, and A. Emami-Neyestanak, "A 18.6-Gb/s Double-Sampling Receiver for Ultra-Low-Power Optical Communication," *IEEE J. Solid-State Circuits*, vol.48, no.2, pp.344-357, Feb. 2013.

[10] T. Huang, T. Chung, C. Chern, M. Huang, C. Lin, and F. Hsueh, "A 28Gb/s 1pJ/b shared-inductor optical receiver with 56% chip-area reduction in 28nm CMOS," *IEEE Intl. Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC)*, pp. 144-145, 2014.

[11] Q. Pan, Z. Hou, Y. Wang, Y. Lu, W. Ki, K. C. Wang, and C. P. Yue. "A 48-mW 18-Gb/s fully integrated CMOS optical receiver with photodetector and adaptive equalizer." in *IEEE Symp. VLSI Circuits Dig. Of Tech. Papers*, pp. 1-2, 2014.

[12] J. Jiang, P. Chiang, H. Hung, C. Lin, T. Yoon, and J. Lee, "100Gb/s ethernet chipsets in 65nm CMOS technology," in *IEEE Intl. Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC), pp. 120-121,* 2013.

[13] D. Kucharski, D. Guckenberger, G. Masini, S. Abdalla, J. Witzens, and S. Sahni, "10Gb/s 15mW optical receiver with integrated Germanium photodetector and hybrid inductor peaking in 0.13µm SOI CMOS technology," in *IEEE Intl. Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC)*, pp. 360-361, 2010.

[14] M. Rakowski, M. Pantouvaki, P. De Heyn, P. Verheyen, M. Ingels, H. Chen, J. De Coster et al., "A 4×20Gb/s WDM ring-based hybrid CMOS silicon photonics transceiver," *IEEE Intl. Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC)*, pp. 1-3, 2015.

[15] M. Georgas, B. R. Moss, C. Sun, J. Shainline, J. S. Orcutt, M. Wade, Y. Chen et al., "A monolithically-integrated optical transmitter and receiver in a zero-change 45nm SOI process," in *IEEE Symp. VLSI Circuits Dig. of Tech. Papers*, pp. 1-2, 2014.

[16] E. Temporiti, G. Minoia, M. Repossi, D. Baldi, A. Ghilioni, and F. Svelto, "A 3D-Integrated 25Gbps silicon photonics receiver in PIC25G and 65nm CMOS technologies," in *IEEE European Solid-State Circuits Conf. (ESSCIRC)*, pp. 131-134, 2014.

[17] S. Menezo, "Silicon Photonics Toolbox for Tb/s-Class Transceivers" *Boston Chapter of the IEEE Photonics Society*, *MIT Lincoln Laboratory*, April 2015.

[18] M. Nazari, and A. Emami-Neyestanak. "A 24-Gb/s double-sampling receiver for ultra-low-power optical communication." *IEEE J. Solid-State Circuits*, Vol. 48, no. 2, pp. 344-357, Dec. 2013.

[19] Palermo, Samuel, Azita Emami-Neyestanak, and Mark Horowitz. "A 90 nm CMOS 16 Gb/s transceiver for optical interconnects." *IEEE J. Solid-State Circuits*, Vol. 43, no. 5, pp. 1235-1246, May 2008.

Saman Saeedi (S'10) received his double-major B.Sc. degree in electrical engineering and physics from Sharif University of Technology, Tehran, Iran, in 2010. He received the M.S. degree from California Institute of Technology, Pasadena, in 2011, in electrical engineering. He is currently working toward his Ph.D. degree at California Institute of Technology, Pasadena. The focus of his current research is low-power, high-performance mixed-signal integrated circuits, with an emphasis on optical and electrical hybrid integration. During the summer of 2012 he was a display design engineer at Apple Inc. From summer of 2014 he is working at Rockley Photonics where he designs CMOS/Silicon Photonic high-speed optical links.

Mr. Saeedi is a gold medalist of the National Physics Olympiad and recipient of four years undergraduate fellowship from National Elite Foundation of Iran. Mr. Saeedi received the Atwood fellowship in Fall 2010. He is the recipient of 2014 Intel/Texas Instruments/Catalyst Foundation CICC Student Scholarship Award and a finalist of 2015 Broadcom Foundation University Research Competition.

Sylvie Menezo was born in Lyon, France. She graduated from INSA Lyon in material sciences. In 1999, she received the Ph.D. degree in optoelectronics from the Centre National d'Etude des Télécommunications (France Telecom). She then joined Alcatel Corporate Research Center (France), where she completed a transfer of a laser pump to Alcatel Optronics production lines. Besides telecom applications, she has worked on seismic fiber optic sensing applications with the company Sercel (Compagnie Générale de Géophysique) for 8 years where she set up and led the "Optical technologies" R&D lab (France & USA).

She joined CEA-Leti (France) in 2010, having, as main topics of research, design and prototyping of optical communication links based on Silicon Photonics devices and CMOS electronic circuits. She led the Silicon photonics lab at CEA-Leti for 2 years (2012-2013) and she is now the Head of Integrated Photonics Programs at CEA-Leti, and Director of the IRT Nanoelec Photonics Program that brings together, under a single roof, expertise and equipment addressing the entire photonics-on-silicon value chain. Mentor Graphics, ST Microelectronics, CNRS, SAMTEC, and CEA-Leti are core members of this consortium.

Gabriel Pares has an Engineer degree in material science from l'Institut National des Sciences Appliquées (INSA) de Lyon, France and a post graduate degree in semiconductor material sciences from the University of Lyon. He has been working for 23 years in semiconductor and MEMS industry in industrial and R&D fields, formerly for STMicro and MEMScap, then he joined CEA-leti in 2004.

He is currently project leader at CEA-Leti in the Laboratory of Packaging and Integration, working on 2.5D/3D chip stacking, Silicon interposer, TSV integration as well as rebuilt wafer technologies and advanced packaging solutions. Additionally, he is in charge of the Open3D platform providing access to 3D technologies for Leti's customers. He holds 4 patents in 3D integration fields.

Azita Emami (S'97–M'04) was born in Naein, Iran. She received the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1999 and 2004, respectively. She received the B.S. degree with honors from Sharif University of Technology, Tehran, Iran, in 1996.

She is currently a Professor of electrical engineering at the California Institute of Technology, Pasadena, CA. From July 2006 to August 2007, she was with Columbia University, New York, NY, as an Assistant Professor in the Department of Electrical Engineering. She also worked as a Research Staff Member at IBM T. J. Watson Research Center, Yorktown Heights, NY, from 2004 to 2006. Her current research areas are high-performance mixed-signal integrated circuits and VLSI systems, with the focus on high-speed and low-power optical and electrical interconnects, clocking, biomedical implant and compressed sensing.