

An 8GHz First-order Frequency Synthesizer based on Phase Interpolation and Quadrature Frequency Detection in 65nm CMOS

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Abstract — A low-power high-speed frequency synthesizer in 65nm CMOS is presented. The design features a novel architecture combining an LC quadrature VCO, two sample-and-holds, a phase interpolator, digital coarse-tuning and a novel quadrature frequency detection technique for fine-tuning. The system works based on injecting the rising edges of reference clock. The architecture has first-order dynamics, eliminating jitter accumulation. Functionality of the frequency synthesizer was validated between 8-9.5GHz, LC VCO's range of operation. The output clock at 8GHz has an integrated rms jitter of 0.5ps and peak-to-peak periodic jitter of 2.9ps. The reference spurs are -64.3dB below the carrier frequency. The system consumes 2.49mW from a 1V supply at 8GHz.

Index Terms — Analog-digital integrated circuit, hybrid integrated circuits, interpolation, phase-locked loops.

I. INTRODUCTION

On-chip frequency synthesizers are one of the main bottlenecks towards faster and lower-power VLSI circuits. Programmable frequency synthesizers, in forms of delay locked loop (DLL) and phase locked loop (PLL), are widely used for high frequency on-chip clock generation as well as high-speed transceivers. As the frequency of operation gets higher and jitter and skew budgets get more limited, requirements for clock phase noise get tighter. Traditional frequency synthesizers have a multiplying PLL (MPLL) architecture, which often has a second order loop and suffers from jitter accumulation. Besides, in traditional architectures phase-frequency detector (PFD) delay mismatch and charge pump (CP) mismatch induce systematic jitter. More recent architectures incorporate a first order loop of multiplying delay locked loop (MDLL) [1], [2], [5]. MDLL's tend to have better performance since they are first order and they inject the rising edge of the reference clock to the line, cleaning any jitter left from the past. However, MDLLs still suffer from high power consumption, limited speed and mismatch in PFD and CP. Moreover, the logic block that generates a select pulse, which opens an aperture for reference injection, limits jitter performance and the maximum output frequency [1], [2]. The proposed frequency synthesizer resolves many of these issues. Phase-interpolator based reference injection, allows high frequency output and low jitter and the proposed first order frequency detection is insensitive to

charge pump mismatch or process variation. This system has a first order loop dynamic, eliminating jitter accumulation. Unlike MDLLs, the new first order architecture can utilize both LC oscillator and inverter-based ring oscillator, depending on application and jitter requirements. In the prototype presented in this paper an LC VCO has been used for low phase-noise demonstration.

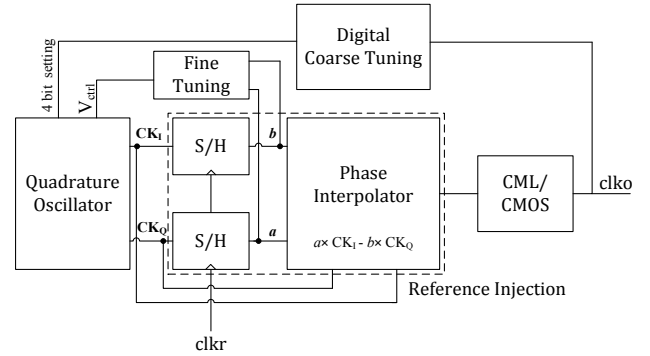


Fig. 1. Top-level architecture of the proposed frequency synthesizer.

Performance of frequency synthesizers is highly dependent on the quality of their reference clock. In addition to electrical reference clock, the prototype chip is capable of receiving a low jitter optical reference clock generated by high-repetition rate mode-locked lasers [7].

The proposed frequency synthesizer was implemented in a 65nm CMOS technology. It operates with a reference clock in the range of 400MHz to 1GHz to generate an output signal in the range of 8-9.5GHz. The frequency synthesizer can be programmed to multiply the frequency by any value between 8-32, as long as the reference clock frequency and output clock frequency fall within ranges mentioned above. The prototype is fully tested with electrical reference clock and its performance is measured. This paper is organized as follows. Section 2 explains the overall system architecture and principles of operation. Section 3 covers the circuit details of different building blocks. In section 4 measurement results are presented, and section 5 is the summary and conclusion of the paper.

II. SYSTEM ARCHITECTURE AND PRINCIPLES OF OPERATION

Fig. 1 shows the top-level architecture of the frequency synthesizer. The basic operation of this system can be broken into three elements. The reference clock injection restarts the phase at every rising edge of the reference clock. The coarse-tuning forces the output clock to have exactly M rising edges in one reference clock period; and the fine-tuning tunes the output frequency to be exactly

$$f_{out} = M \times f_{ref}. \quad (1)$$

The coarse and fine-tuning blocks are always operational in the loop and correct any error instantly.

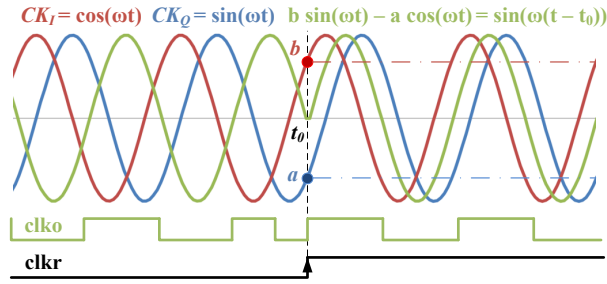


Fig. 2. Injection of the reference clock rising edge through sampling and phase-interpolation.

The phase-interpolator-based reference injection technique is shown in Fig. 2. A rising edge at t_0 updates the value of a and b , samples taken from CK_I and CK_Q respectively. The updated values of a and b are interpolated with CK_Q and CK_I as

$$CK_{out} = a \times CK_Q - b \times CK_I. \quad (2)$$

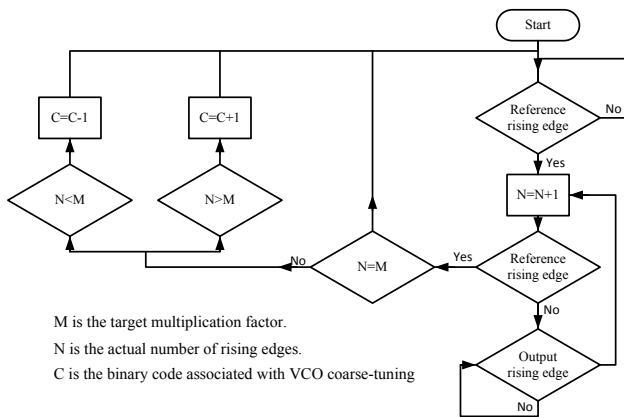


Fig. 3. Digital coarse-tuning block flow-chart.

As shown in Fig. 2 phase of CK_{out} is now reset at t_0 , regardless of the phase of CK_I and CK_Q . This technique

has been previously used in the burst-mode CDR in [5]. The flow chart in Fig 3 demonstrates the operation of coarse-tuning block. The coarse-tuning is a low power digital system with two counters and two comparators. It counts the number of rising edges of output clock in each reference clock period, and compares it to the target multiplication factor. The output of the comparator changes the capacitance of quadrature oscillator's LC tank accordingly, adjusting its frequency of operation. Since the phase-interpolator injects the rising edge of the reference, the output can have the same number of rising edges for a range of input frequencies. A new quadrature frequency detection technique is used for fine-tuning and it is shown in Fig. 4. The principle of fine-tuning is based on the beat frequency and phase difference of samples taken from CK_I and CK_Q . These samples have a beat frequency of

$$f_{beat} = |f_{out} - Mf_{ref}|, \quad (3)$$

providing a reliable measure for deviation of the signal from frequency of interest. The sampled signals from CK_I and CK_Q always have a phase difference of 90° . When $M \times f_{ref} > f_{CK}$, samples taken from CK_Q ($CK_{Q,S}$) lag samples taken from CK_I ($CK_{I,S}$). On the other hand, when $M \times f_{ref} < f_{CK}$, $CK_{I,S}$ lags $CK_{Q,S}$.

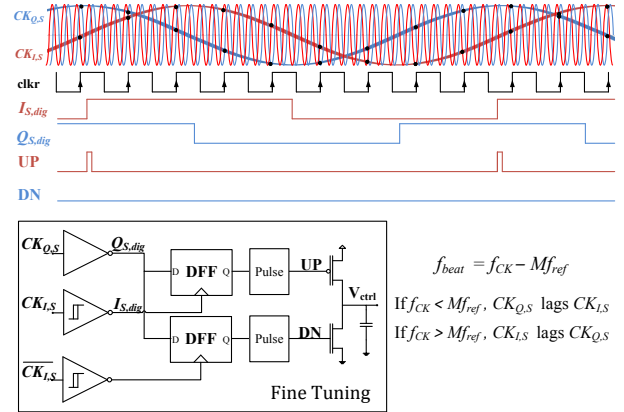


Fig. 4. Principle and implementation of fine-tuning technique.

In this design D flip-flops are used to determine the phase relationship between $CK_{I,S}$ and $CK_{Q,S}$. By extracting the phase information of $CK_{I,S}$ and $CK_{Q,S}$, bang-bang UP/DN pulses associated with each case are generated to increase and decrease the fine-tuning control voltage of LC quadrature VCO. The system behaves as a first order system since frequency corrections are proportional to deviation of output frequency from M times frequency of the reference clock. Schmitt triggers are used to prevent metastability and unwanted pulses when frequency of

oscillator is close to M times frequency of the reference clock. Note that, unlike conventional PFDs, where UP/DN signals turn on at the same time, in quadrature frequency detection UP/DN signals are independent. Therefore, quadrature frequency detection has lower power consumption and is less prone to UP/DN current mismatch. The speed of fine-tuning is limited by the sample-and-hold (S/H) bandwidth.

III. CIRCUIT DESCRIPTION AND BUILDING BLOCKS

Fig. 5 shows the transistor-level implementation of the main building blocks. Fig. 5 (a) shows the quadrature oscillator used in the system with 4 coarse-tuning bits and fine-tuning control voltage. Fig. 5 (b) shows the differential phase interpolator architecture. Clock samples as well as quadrature waveforms are differential to minimize supply noise and phase mismatches. Fig. 5 (c) shows the master-slave S/H implementation. The S/H is designed to have maximum bandwidth and linearity. Non-linearity of S/H induces jitter at the output of the phase-interpolator. Source degeneration is used to reduce non-linearity and minimize output systematic jitter.

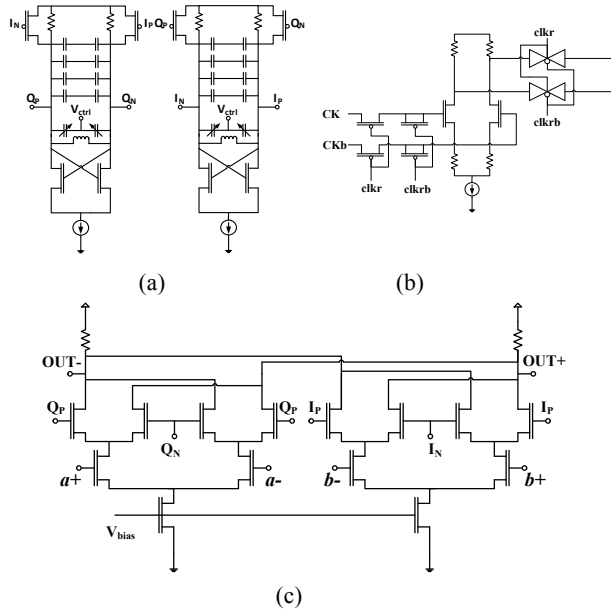


Fig. 5. Transistor-level schematic of main building blocks. (a) LC quadrature VCO (b) master-slave sample-and-hold (c) differential phase-interpolator.

Fig. 6 shows electrical/optical reference generator. A MUX chooses between the two signals. The electrical reference generator, which is used during the test, is simply a CML/CMOS circuit retrieving the signal from an off-chip source. The optical reference generates sharp

rising edges from high-repetition rate mode-locked laser. A tunable feedback circuit resets the voltage before the next pulse arrives. An on-chip tunable RC delay controls the duty-cycle of the reference waveform. Since only the rising edge of the reference is injected to the output clock the duty-cycle and jitter of the falling edge do not play a role in the quality of the output clock.

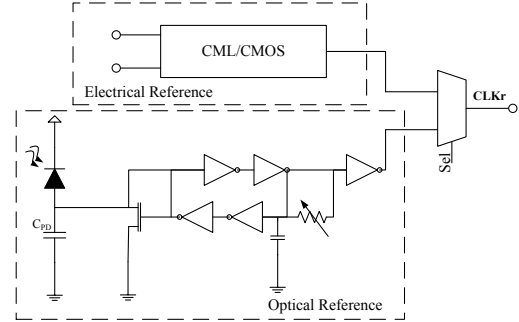


Fig. 6. Electrical/optical reference generator.

IV. TESTING AND MEASUREMENT RESULTS

The proposed frequency synthesizer was fabricated in 65nm CMOS technology. Fig. 7 shows real-time transient response of the system at 8GHz while locking to a 400MHz reference clock. Operation of the phase interpolator at the rising edge of the reference clock can be seen at 3 different times. Frequency of the quadrature VCO changes until lock is acquired. The frequency synthesizer has an operating range of 8-9.5GHz limited by LC VCO's frequency range

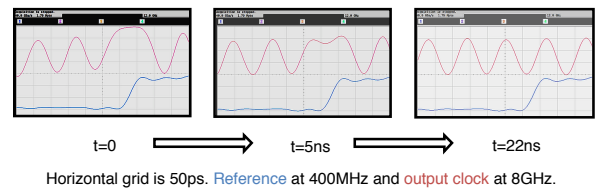


Fig. 7. Real-time lock acquisition measured for a reference clock of 400MHz and output clock of 8GHz.

Jitter performance and reference spurs measurements of the system are shown in Fig. 8 (a) and (b). The output clock has an integrated rms jitter of 0.5ps and periodic peak-to-peak jitter of 2.9ps. Reference spurs are measured to be 64.3dB lower than main frequency.

Fig. 9 shows the power consumption and energy efficiency of the frequency synthesizer while operating at different frequencies. Energy efficiency of the frequency synthesizer is 0.312mW/GHz at 8GHz, which drops to 0.305mW/GHz at 9.5GHz. As the frequency of operation increases, power consumption increases linearly primarily

due to the power consumption of digital elements. The power consumption measurement includes LC quadrature oscillator, sample-and-holds, phase interpolator, coarse-tuning, fine-tuning and output CML-to-CMOS converter.

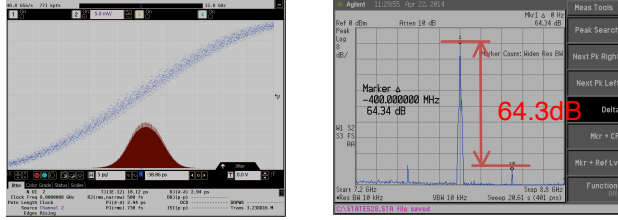


Fig. 7. Jitter performance, histogram and reference spur measurements with electrical reference clock.

Fig. 10 shows the chip micrograph. The frequency synthesizer occupies an active area of 0.044mm^2 including the inductors. Table 1 summarizes performance of the frequency synthesizer and compares it to the state-of-the-art.

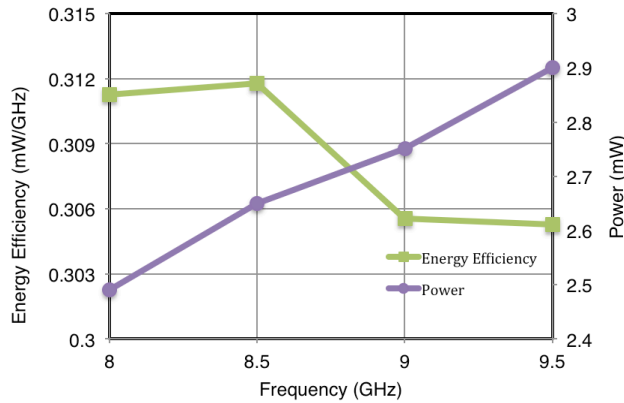


Fig. 9. Power consumption and energy efficiency of the frequency synthesizer at different operating frequencies.

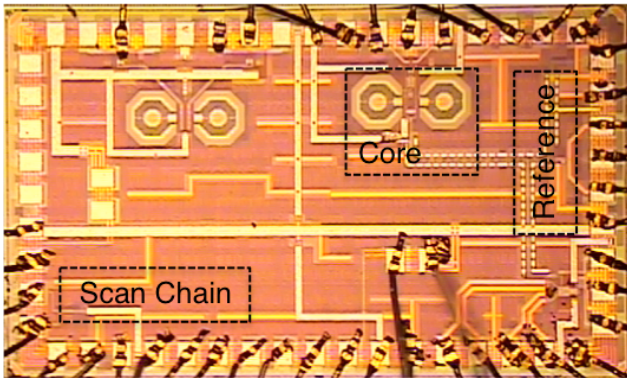


Fig. 10. Die micrograph of the prototype chip.

VII. CONCLUSION

The presented first-order frequency synthesizer operates in the range of 8-9.5GHz and consumes 2.49mW while operating at 8GHz with a multiplication factor of 20 and exhibits 0.5ps rms integrated jitter and 2.9ps peak-to-peak periodic jitter. The reference spurs are measured to be 64.3dB below the carrier frequency. The total active area including inductors is 0.044mm^2 . Experimental results validated functionality of the system with an electrical input clock. This architecture is also well suited for optical clocking using hybrid-integrated photonics and electronics.

Table 1. Performance summary and comparison.

	This Work	[2]	[3]	[4]	[6]
Technology	65nm	90nm	32nm	40nm	65nm
Output Frequency [GHz]	8-9.5	4.6	26.7	5.83	1.6
Reference Frequency [MHz]	400-1000	395	400	26	40-300
Reference Spurs @1MHz [dBc]	-64	-46	-96.3	-102	-40
Jitter rms/PP [ps]	0.5/9.2	2/17.8	-	0.3/-	0.7/-
Power [mW/GHz]	0.312	1.48	3.32	2.56	0.606
Area [mm²]	0.044	0.025	-	0.29	0.022
Method	Novel	MDLL	MPLL	MPLL	MDLL

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