

# A Wideband Injection Locking Scheme and Quadrature Phase Generation in 65nm CMOS

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**Abstract** — A novel technique for wideband injection locking in an LC oscillator is proposed. PLL and injection locking elements are combined symbiotically to achieve wide locking range while retaining the simplicity of the latter. This method doesn't require a phase frequency detector or a loop filter to achieve phase lock. 13.4GHz – 17.2GHz locking range and an average jitter tracking bandwidth of up to 400 MHz was measured in a high- $Q$  LC oscillator. This architecture is used to generate quadrature phases from a single clock without any frequency division, and to provide high frequency jitter filtering while retaining the low frequency correlated jitter essential for clock forwarded receivers.

**Index Terms** — injection-locked oscillator, injection-locked phase-locked loop, locking range, quadrature, jitter transfer function, voltage-controlled oscillator (VCO).

## I. INTRODUCTION

Injection-locked-oscillators (ILOs) have been used in many wireline receivers because of their simple implementation and instantaneous locking characteristics. However, their application is hindered by their limited locking range compared with alternative techniques such as phase-locked-loops (PLLs). Recent standards [1], require operation with data rates that span more than 10% of the nominal frequency. Transceivers must operate reliably over this range. Intricate frequency-tracking mechanism such as a reference PLL has been used before to set the oscillator's natural frequency so that it is within the injection range of the reference clock [2]. This adds additional design complexity and an area/power penalty to the otherwise simple circuit, thus offsetting the merits of injection-locked based system.

Another important requirement of wireline receivers that employ half-rate and quarter-rate architectures is generation of accurate quadrature phases. Injection-locked LC dividers have been frequently used for generating quadrature phases [3], but they require complementary clocks at twice the desired frequency, which tends to be power inefficient. Quadrature phase generation from a single phase of clock without any frequency division is highly desirable for half-rate and quarter-rate CDR architectures.

In this paper we propose a method for wideband injection locking in an LC oscillator that maintains the

simplicity of an injection locked system. We also describe an extension of this method to produce quadrature phases from a single reference clock without any frequency division. The system has a wide jitter tracking bandwidth, which makes it useful for clock forwarded receivers [4].

## II. ARCHITECTURE

In most LC oscillators, the control voltage of the varactor is used to set the frequency of oscillation,  $f_0$ . In such architectures the instantaneous voltage oscillation at the output node results in transient changes in the capacitance (Fig. 2). Due to this effect, the voltage of the common-node (A) has an extra frequency component at  $2f_0$  [5]. Similarly, if we inject a  $2f_0$  component at the varactors' common node, then the mixing action of the varactors will inject a current at  $f_0$  into the tank. However, such circuit will constitute a frequency divider, which is not desirable in many applications. In this section we describe the basic principles of the proposed architecture that avoids such division and provides a very wide locking range.

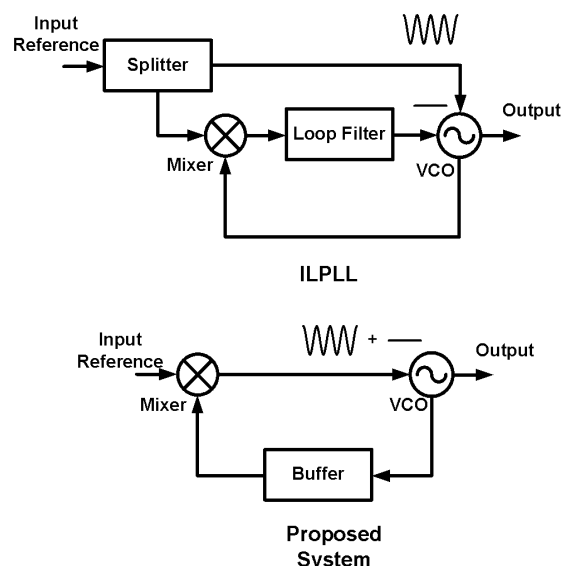


Fig. 1. Block diagram of ILPLL and proposed system

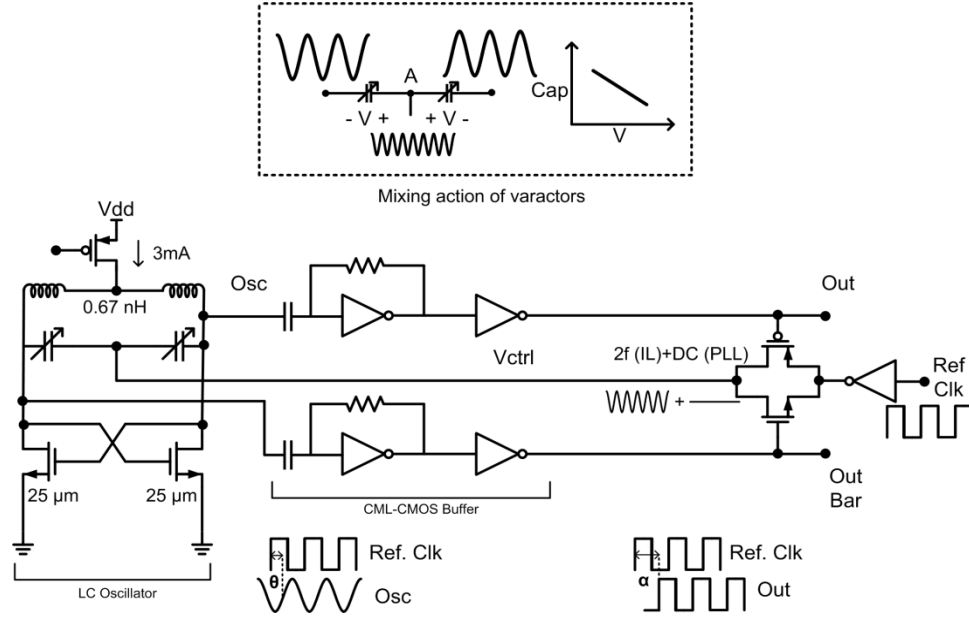


Fig. 2. Schematic of the proposed system. The input to the common mode of the varactors contains  $2f$  and DC component. DC component brings the natural frequency close to the frequency of the reference clock and the  $2f$  component does the injection lock.

In the locked state, an ILO can be modeled as a first-order PLL. A first-order PLL comprises of a VCO, a mixer and a low pass filter. In this work we propose to eliminate the loop filter altogether. The resultant high frequency component of the mixer is used to perform injection locking. This is different from an ILPLL structure (Fig. 1), which consists of a full PLL with additional injection in the VCO to improve its phase noise characteristics. Additionally, unlike the ILPLL both IL and PLL actions are performed at the same node.

Fig. 2 shows the basic schematic of the proposed wideband injection locking system. A complementary transmission gate is used as a single balanced passive mixer. The output of the LC oscillator is buffered by CML to CMOS stage. The transmission gate is driven by the outputs of the buffer and the reference clock is used as the input. The output of the transmission gate is directly fed to the varactors in the LC oscillator. In the locked state the output of the transmission gate contains high frequency  $2f$  component and a DC component. The value of the DC component is determined by the phase difference between the reference and output of the buffer ( $\alpha$ ) and is proportional to  $\cos(\alpha)$  (Fig. 3(d)). The phase difference between the oscillator output and the injected clock ( $\theta$ ) is given by  $\sin(\theta) = (\omega_o - \omega_{inj}) / \omega_L$  [6]. Assuming a constant delay  $\Delta$  through the CML to CMOS buffer, the phase difference between the clock and buffer output  $\alpha = \theta + \Delta \times (2\pi f)$ . So the DC component of the switch output is

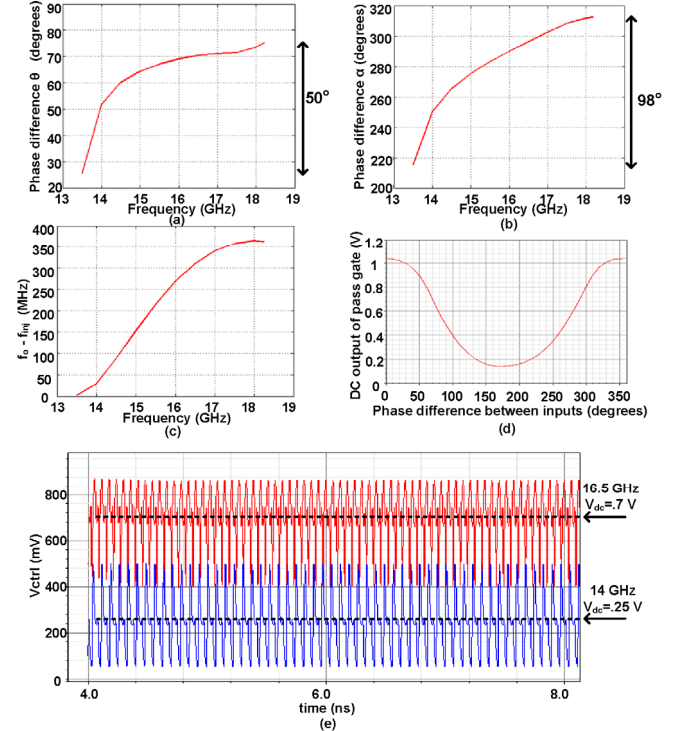


Fig. 3. Simulation results, (a)  $\alpha$  vs. ref. frequency, (b)  $\theta$  vs. ref. frequency, (c)  $f_o - f_{inj}$  vs. ref. frequency, (d) DC characteristic of the transmission gate, (e) Vctrl at 14GHz and 16.5GHz clock reference

dependent on  $\theta$ . In the unlocked state, the DC component brings the  $f_o$  close to  $f_{inj}$  (PLL action) and the  $2f_{inj}$  component performs the injection lock. Thus the phase difference  $\theta$  becomes dependent on reference frequency, which enables wideband locking. Fig. 3(e) shows the simulated varactor control voltages under locked condition for two frequencies (14GHz and 16.5GHz). The DC levels are different and are overridden by the corresponding  $2f_{inj}$  components.

Fig. 3 (a) shows the simulated oscillator output phase difference ( $\theta$ ) versus input frequency.  $\theta$  is smaller at lower frequencies and it increases as frequency increases. This is in accordance with the DC characteristic of the transmission gate (Fig. 3 (d)) and phase difference between the CML to CMOS output and the reference clock ( $\alpha$ ). The fact that CML to CMOS buffers add a constant delay across all frequencies helps increase the injection range as it amplifies the phase shift when frequency increases ( $\alpha = \theta + \Delta \times (2\pi f)$ ). This helps the switch output to cover the entire voltage range (0-Vdd), shown in Fig. 3(d).

For quadrature phase generation a secondary matched LC oscillator is coupled to the primary in a QVCO configuration (Fig. 4). The control voltage of the secondary is generated from the output of the transmission gate after sending it through a passive low pass filter, consisting of two RC sections in series with  $R=1k\Omega$  and  $C=80fF$ . Thus both oscillators have the same  $f_o$ . The oscillation phase of the replica oscillator can be adjusted by changing the bias of the varactors VarA and VarB which are chosen to be more than 7 times smaller than the main varactors (Fig. 4), enabling compensation for polarized-mode dispersion effects.

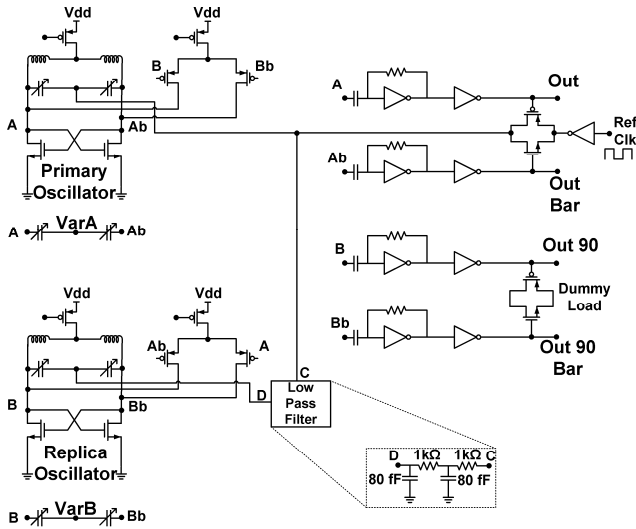


Fig. 4. Schematic of the proposed system for quadrature phase generation.

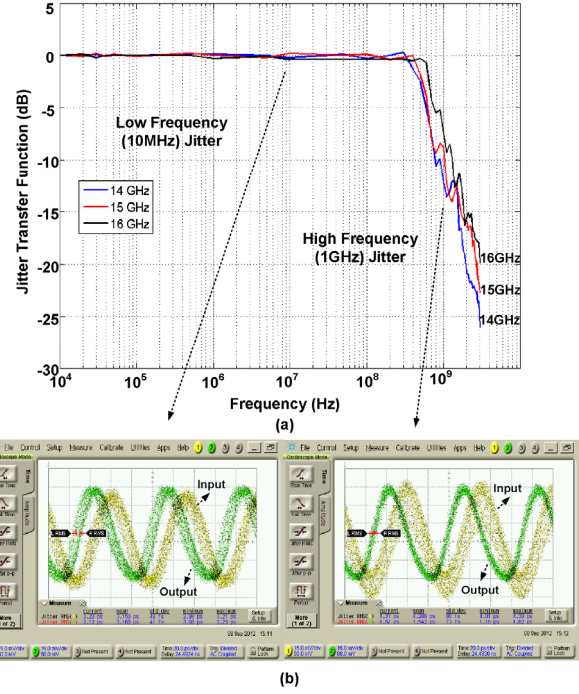


Fig. 5. (a) Measured Jitter transfer function for 14GHz, 15GHz and 16GHz reference frequencies, (b) Response to low frequency (10MHz) and high frequency (1GHz) jitter

### III. MEASUREMENT RESULTS

A prototype has been designed and fabricated in 65nm CMOS technology, with a 1V supply voltage. nMOS transistors in accumulation mode are used to implement the varactors with control voltage applied to the drain/source. Spiral inductors of value 0.67 nH are designed to have maximum simulated  $Q$  of 14 in the frequency range of interest. They are constructed using thick, top two metal layers with added ground mesh for  $Q$  enhancement. A high- $Q$  design was chosen to substantiate the efficacy of the proposed locking range extension technique as injection locking range is inversely proportional to  $Q$  in standard ILOs [6]. A reference clock from an external signal source is used for injection. A locking range of 13.4GHz – 17.2GHz was measured, which translates to 24.8% around the center frequency. The achieved locking range is limited by the varactor tuning range. The average power consumption was 9 mW for the entire system. For comparison, a previous design [7], uses a low- $Q$  (2.5) inductor to achieve a maximum locking range of 12% with strong injection while consuming 13.1 mW for a single injection locked LC oscillator.

The rms jitter values across several frequencies in the locking range are plotted in Fig. 6(a). A maximum rms

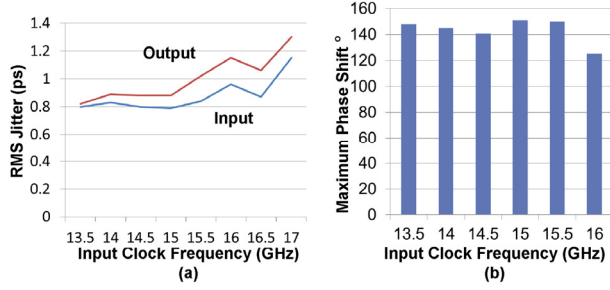


Fig. 6. (a) Measured Input and Output Jitter at different reference frequencies, (b) Measured maximum phase shift of the replica oscillator

jitter addition of 0.15 ps is observed at 17 GHz, which is expected considering that system output goes through several buffers to drive the output stage. To measure the jitter transfer function, the phase of the reference clock was modulated and the spectrum components of the output were measured at the carrier and sideband frequencies. Jitter transfer function (Fig. 5 (a)) was measured for three reference frequencies (14GHz, 15GHz and 16GHz), and an average jitter tracking bandwidth (JTB) of 400 MHz was recorded. High JTB helps in retaining the low frequency jitter while eliminating high frequency jitter as depicted in Fig. 5(b). It is important to retain the low frequency jitter in clock forwarded receivers as low frequency jitter is correlated with the data [4]. Quadrature phase accuracy was confirmed by measuring the phase difference between the two outputs after careful calibration of the measurement setup. A maximum offset of 2.8% (from 90°) is observed between the two phases at 15GHz. Bias to VarA and VarB were fixed while making quadrature accuracy measurements. They were then varied from 0-V<sub>dd</sub> to measure the maximum phase shift of replica oscillator (Fig. 6(b)).

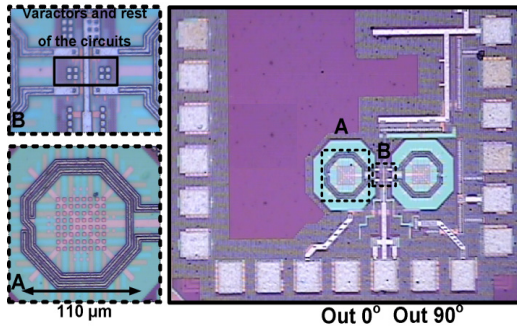


Fig. 7. Die Micrograph

#### IV. CONCLUSION

In summary in this paper a new locking scheme for extended injection range is introduced. It requires only a

single clock phase for operation. Quadrature phase generation is demonstrated by adding a secondary coupled oscillator to the system. This wide locking range of the proposed system eliminates the need for center-frequency adjustment.

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TABLE I  
SUMMARY OF PERFORMANCE

Process technology	65nm CMOS
Injection range	13.4GHz – 17.2GHz
RMS Jitter In-Out (13.5 GHz)	0.80 ps - 0.82 ps
Average Jitter Tracking BW	400 MHz
Active Area	0.3 x 0.11 mm <sup>2</sup>
Supply voltage	1V
Average Power Consumption	9 mW (LC oscillators 65 % and buffers 35 %)

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