16.6 A Fully Intraocular 0.0169mm²/pixel 512-Channel Self-Calibrating Epiretinal Prosthesis in 65nm CMOS

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Since their conception and success in human trials, the flexibility and spatial resolution of retinal prostheses have been of major interest. Clinical studies have revealed that hundreds of channels are needed to restore functional visual perception [1], and more sophisticated waveforms present advantages over biphasic pulses [2]. Initial designs targeted stimulation current levels up to 1mA to ensure functionality. For such designs, an output compliance of >10V was required [2,3], and HV technologies were used at the expense of area and power consumption [2-6]. Human clinical trials have recently shown that implanted electrodes present a stimulus threshold as low as 50μA [1]. In addition, advances in implant technology promise close placement of electrode array and retinal tissue, which can further decrease the required current. Thus, highly scaled LV technologies can provide alternative means to reduce area and power, and to support hundreds of flexible independent channels for fully intraocular implants. In this paper, a self-calibrating 512-channel epiretinal prosthesis in 65nm CMOS is presented. It features dual-band telemetry for power and data, clock recovery, a 2-step calibration technique to match biphasic stimulation currents, and an independent arbitrary output waveform per channel. The implant integrates coils (power and data), IC, external capacitors and electrode array using a biocompatible parylene substrate, providing a fully intraocular solution.

The system architecture is shown in Fig. 16.6.1. The power telemetry operates at 10MHz and produces four different voltage levels: $\pm 2V_{dd}$ for stimulation and $\pm V_{dd}$ for the rest of the system. The rectifier (Fig. 16.6.2) utilizes transistor-based diodes and unidirectional switches to prevent reverse conduction loss in the power transistors, improving its efficiency to more than 80% while delivering ≈25mW. Its output (V_{rec}) is used by DC-DC converters to generate $-V_{rec}$ and $\pm 2V_{rec}$, which are regulated to produce the supplies. The DC-DC converters and LDO regulators present >90% and >85% efficiencies, respectively, for a total efficiency of 65%. The supplies are measured to be ≈±1.3V and ≈±2.5V. The data receiver is a pseudo-differential PSK demodulator with gain control to support up to 20Mb/s of data. The 10MHz power signal is used as a reference by the PLL to generate I/Q 160MHz clocks for down-conversion and a 20MHz clock for data slicers. The datapath and PLL consume 2.3mA and 350μA respectively. The stimulator array is composed of 512 independent channels grouped into 8 blocks. The global logic receives and demultiplexes the data for each block. The only off-chip components in this design are capacitors and power/data coils.

The architecture of the stimulator is shown in Fig. 16.6.2. To enable robust operation with high output voltage, low-headroom current mirrors and protection transistors are used in the current driver. Using 1.2V core and 2.5V I/O transistors, a 5V output stage is designed. Accumulated charge from the body effect in the protection transistors is removed via a switch prior to stimulation. The local logic is shared between 4 channels and controls the stimulation and calibration. It uses a low-frequency clock (10kHz) and consumes <1μW. A specific waveform is generated by sending a data sequence that defines the amplitude of the waveform every 100μs with 4b of resolution. Anodic and cathodic phases are used to inject or remove charge from the tissue. Any remaining charge imbalance is removed during a discharge phase, when the electrode is shorted to ground. Figure 16.6.3 shows measurements of arbitrary waveforms generated by the chip using a 75μm/300μm inner/outer diameter Pt/Ir flat concentric bipolar electrode in 1X PBS solution as a load while the implant receives power and data wirelessly. V_{outmax} is measured to be ±2.4V.

Matching the current or charge of biphasic stimulation is an important design consideration in retinal implants. Analog techniques to sample correction currents [5,6] require large area and rely on a constant output current that limits them to biphasic pulses. Active charge balancers [2,4] keep the residual tissue charge within a safety window, but such compensation depends on the output waveform and changes for different wave shapes. In addition, both techniques have to run for every stimulation. In this work, we propose a digital calibration method to match anodic (I_{pmos}) and cathodic (I_{nmos}) currents. The calibration needs to run only once when the implant is turned on (e.g. daily). Figure 16.6.4 shows the proposed 2-step calibration scheme. During the first step, the offset of I_{nmos} (current value at zero input) is cancelled. Second, I_{pmos} is matched to I_{nmos} by reducing their difference (I_{diff}). Since the slope of the two currents can vary, reducing I_{diff} at one point will not match them over the entire range. This problem can be removed if the output current range is split into regions and a distinct calibration is done for each region. In this design, for the target mismatch of <5%, a 5-point calibration scheme is chosen.

The calibration proceeds as follows: Two switched resistors R_H and R_L (Fig. 16.6.2) are used to sense I_{out} during calibration. R_H (high resistance) increases the conversion gain when I_{out} is low, while R_L (low resistance) ensures voltage compliance when I_{out} is high. To measure the offset of I_{nmos} (step 1), a zero input is set, R_H is connected to the output, I_{nmos} is turned on and the voltage across the resistor is compared to $V_{ref}=-I_{bcal}*R_b$ (Sel=0). Based on this, the calibration current ($I_{calnmos}$) is changed to adjust I_{nmos} until the comparator switches. Then, the value of the calibration DAC is stored in a local register. To measure I_{diff} (step 2), R_L is connected and both currents are turned on so that I_{diff} flows to R_L. Using the same method with V_{ref}=0V, a correction current ($I_{calpmos}$) is added to I_{pmos}. Variations on R_H, R_L, R_b, I_{bcal} and I_{refcal}, as well as offset of comparator and preamplifier set the resolution of the calibration. To maximize current matching, resistors are carefully sized so that $V_{LSB} = (I_{refcal} \times R_{H/L})_{min} > (I_{bcal}*R_b)_{max} + \Sigma V_{offset}$. Thus, the I_{refcal} variation is the dominant factor. This variation is minimized by proper sizing of transistors in the bias network at the expense of slightly higher power consumption. Measurements of current matching are shown in Fig. 16.6.4. A 10× improvement on I_{diff} is achieved when the calibration is turned on. A statistical measurement over 40 channels from 5 different chips presents a current mismatch with mean of 1.12μA and standard deviation of 0.53μA. While the calibration circuitry is shared among every 4 channels, each channel is calibrated independently.

Figure 16.6.5 shows the chip-parylene integration and the 3-coil scheme for efficient inductive power transmission [7]. The flexible MEMS intraocular origami coil has a Q of ≈24 at 10MHz, 10mm outer diameter and 10mg mass in aqueous solution. An efficiency of 36.5% is measured with 1-inch separation in saline. The chip is fabricated in 65nm LP CMOS (Fig. 16.6.7) and occupies an area of 4.5×3.1mm². It consumes 15mW for a 10% duty cycle, 50μA biphasic pulse at 50% activity factor. The 4-channel stimulator occupies an area of 260×260μm² including pads, ESD structures and bypass capacitors (pixel size of 0.0169mm²). The tables in Fig. 16.6.6 summarize the performance and compares it with prior art. The system achieves a reduction of 66.2% in pixel size and 37.78% in current mismatch.

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References:
[1] J. Weiland and M. Humayun, "Visual Prosthesis," *Proc. IEEE*, vol. 96, no. 7, pp. 1076-1084, July 2008.
[2] K. Sooksood, *et al.*, "A Neural Stimulator Front-End with Arbitrary Pulse Shape, HV Compliance and Adaptive Supply Requiring 0.05mm² in 0.35μm HVCMOS," *ISSCC Dig. Tech. Papers*, pp. 306-308, Feb. 2011
[3] K. Chen, *et al.*, "An Integrated 256-Channel Epiretinal Prosthesis," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1946-1956, Sept. 2010.
[4] M. Ortmanns, *et al.*, "A 232-Channel Visual Prosthesis ASIC with Production-Compliant Safety and Testability," *ISSCC Dig. Tech. Papers*, pp. 152-153, 593, Feb. 2007.
[5] E. Lee and A. Lam, "A Matching Technique for Biphasic Stimulation Pulse," *IEEE ISCAS*, pp. 817-820, May 2007.
[6] J. Sit and R. Sarpeshkar, "A Low-Power Blocking-Capacitor-Free Charge-Balanced Electrode-Stimulator Chip With Less Than 6 nA DC Error for 1-mA Full-Scale Stimulation," *IEEE Trans. BioCAS*, vol. 1, no. 3, pp. 172-183, 2007.
[7] Y. Zhao, *et al.*, "High Performance 3-Coil Wireless Power Transfer System for the 512-electrode Epiretinal Prosthesis," *IEEE EMBS*, Sept. 2012.

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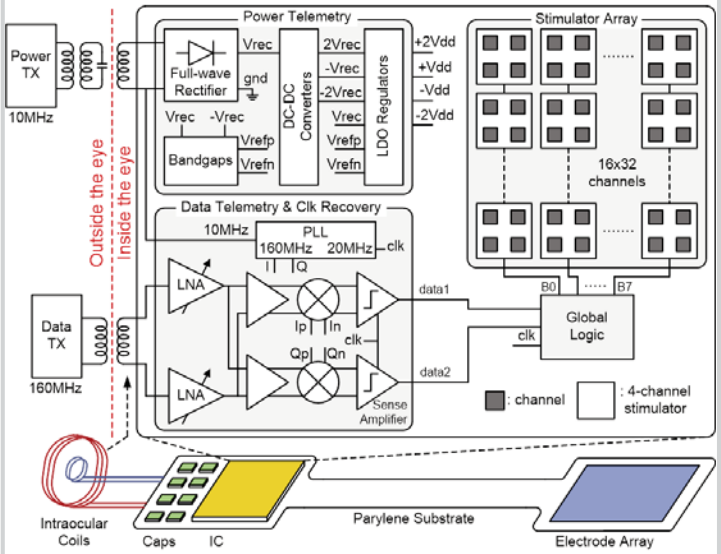


Figure 16.6.1: Fully intraocular epiretinal prosthesis top-level architecture.

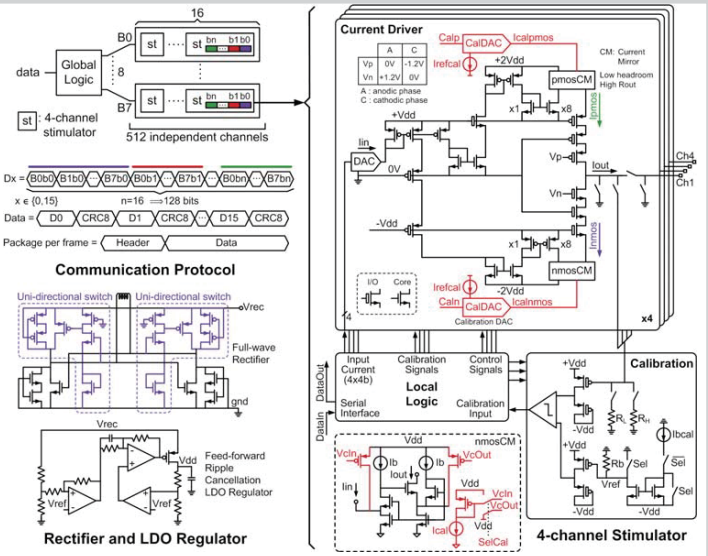


Figure 16.6.2: Communication protocol, rectifier, LDO regulator and 4-channel stimulator. I/O transistors are used only for protection.

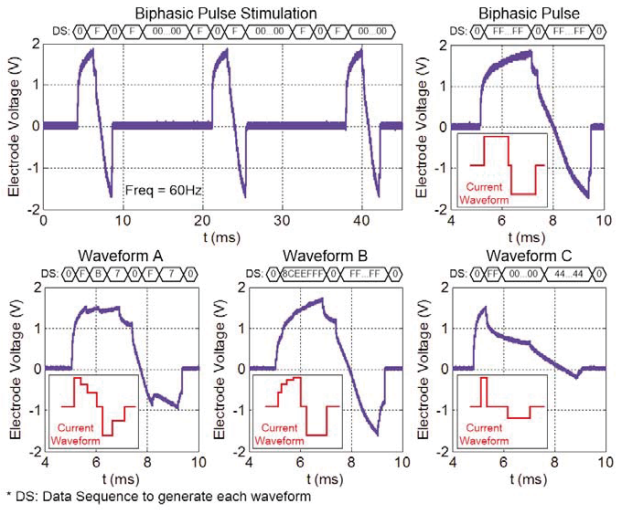


Figure 16.6.3: Measured arbitrary output waveforms using a Pt/Ir flat concentric bipolar electrode in 1X PBS solution as a load while power and data are delivered wirelessly.

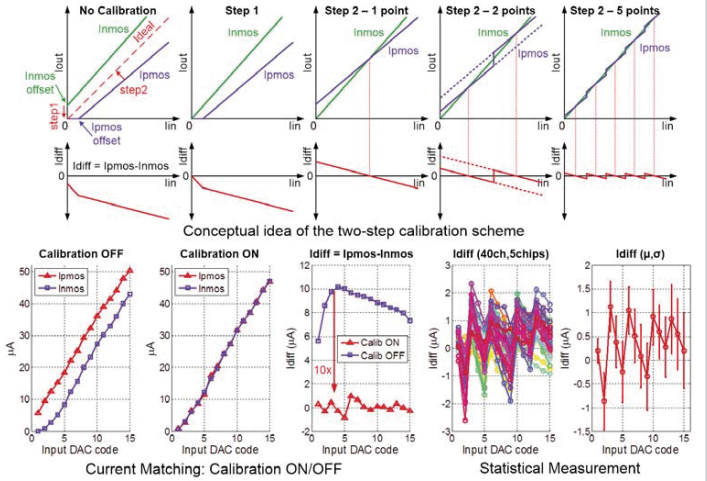
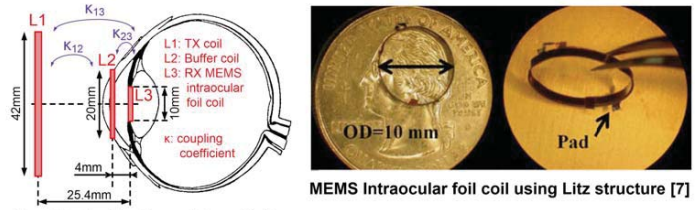
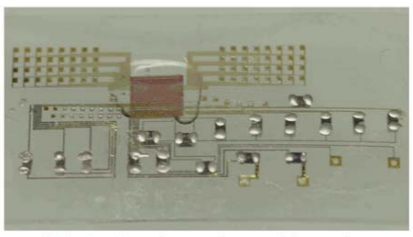


Figure 16.6.4: 2-step self-calibration technique. Measurements of current matching from a single channel show a 10× improvement when calibration is turned on. Statistical measurement over 40 channels from 5 different chips shows μ=1.12μA and σ=0.53μA.

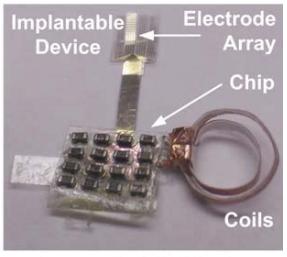


3-coil Inductive Power Tranmission

MEMS Intraocular foil coil using Litz structure [7]



Chip-Parylene integration used for testing



Implantable folded device

Figure 16.6.5: Inductive power transmission using 3-coil scheme, MEMS intraocular foil coil, chip-parylene integration used for testing and prototype of the implantable system.

Performance Comparison: Epiretinal Prosthesis

	[3]	[4]	This Work
CMOS Process	HV 0.18μm	HV 0.35μm	65nm 1.2V/2.5V
Modulation	DPSK @ 22MHz	Photodiode	PSK @ 160MHz
Data Rate	2Mb/s	968kb/s	Up to 20Mb/s
Power Carrier	2MHz	N.A.	10MHz
On-Chip Supplies (V)	±1.8, ±12	3.3, 11.25, 22.5	±1.3, ±2.5
Number of Channels	256	232	512
Iout max (μA)	500	1000	50
Vout range (V)	-10, +10	>20 (1.25, 21.25)	-2.4, +2.4
Pixel Size (mm^2)	0.08034	~ 0.0718	0.0169
Shared Channels	1	2*	1**
Mismatch (μA)	<14.5	<50, charge balancers	μ=1.12,σ=0.53†
Load model	10kΩ+100nF	10kΩ+100nF	30kΩ+100nF
Total Area (mm^2)	5.3 x 5.1	4.9x4.5	4.5 x 3.1††

Performance Comparison: Stimulator

	[2]	[5]	[6]	This Work
CMOS Process	HV 0.35μm	HV 0.5μm	HV 0.7μm	65nm 1.2V/2.5V
Supplies (V)	3, 10, 20	±3, ±8	-9, +6	±1.3, ±2.5
Vout range (V)	0.3, 19.7	-7.45, +7.45	-8, +5	-2.4, +2.4
Pixel Size (mm^2)	0.05	0.51	1.44	0.0169
Shared Channels	4*	1	1	1**
Mismatch (μA)	charge balancers	1.8	4	μ=1.12,σ=0.53†
Load model	10kΩ+100nF	N.A.	3.9kΩ+10nF	30kΩ+100nF

* no independent channels ** every 4 independent channels share local logic and calibration circuitry
† statistical measurement (μ: mean, σ: standard deviation)
†† including extra area for placement in parylene (0.4mm on the bottom, 0.2mm on the sides and top)

Figure 16.6.6: Performance summary and comparison with the prior art. It is important to note that none of the previous work in the literature has reported statistical measurements for current matching.