Capacitive Proximity Communication with Distributed Alignment Sensing for Origami Biomedical Implants

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***Abstract*—Origami implant design is a 3D integration technique which addresses size and cost constraints in biomedical implants. A capacitive proximity interconnect that enables this technique is presented. The interconnect embeds an alignment sensor that measures link quality directly and simplifies its adaptation to alignment. The sensor and transceiver share functional blocks, saving power and area. Data rates from 10-60 Mbps are achieved over 4-12 μm of parylene-C, with efficiencies up to 0.180 pJ/bit.**

I. Introduction

Designers of medical implants face three primary challenges: size, cost and power consumption. At the same time, there is a desire to increase the capability of these implants. For example, recent developments in retinal prosthesis design have targeted as many as 1024 electrodes [1], [2] in order to achieve reasonable visual resolution. Such increases in capability require the development of specialized, highly-integrated system-on-chip designs, which can be cost-prohibitive for low-volume applications typical in the biomedical market. Even with highly-integrated designs, the size of the system required can pose an implantation challenge in small and delicate organs such as the eye; for example, if the design in [1] is scaled up to 1024 electrodes, approximately 8x8 mm^2 is required for the stimulator array alone, excluding power delivery, data telemetry and digital control. Compounding this problem, the high voltages ($\sim$5-10V) typically used to drive the desired stimulus currents prevent the use of finer-geometry process technology.

In order to work around size limits, large systems can be split into multiple chips and connected using 3D integration techniques. For example, they can be placed on a flexible, biocompatible substrate such as Parylene-C [3]. This substrate can be folded compactly for implantation, then unfolded into its operating configuration inside the body, allowing minimally-invasive surgery [4]. Other applications of this Origami folding technique include conforming a retinal prosthesis to the back of the eye to improve electrode contact and make stimulation more effective. This concept can be further extended to address the high cost of developing custom SoC designs for each new implant; electronics can be partitioned into commonly-used functional blocks, mass-produced as ICs that are embedded into parylene library modules. Custom implants can be assembled from these (relatively) cheap modules.

To enable Origami implants, individual ICs will need to be able to communicate with each other wirelessly. Proximity communication [5] provides a compelling way to achieve this, thanks to its low cost of integration and the fact that many of the ICs in an Origami implant can be placed close to each other and face-to-face. However, existing approaches to proximity communication have targeted multi-Gbps links in high-performance computing [6] and memory-stacking [7] applications, and so have been designed under a different set of constraints than the relatively low data rates and ultra-low power consumption required by implants.

II. Proximity Communication For Origami Implants

Since the Origami implant is deployed in-body, the alignment between the communicating chips is poorly controlled. Furthermore, the alignment will change over time due to patient movement and tissue growth. As a result, the proximity communication system needs to periodically sense its alignment and adapt itself to maximize power efficiency for a given data rate. Alignment sensing is also useful for providing feedback on the deployment status of the implant. Due to the tight power constraints on implants in sensitive organs such as the eye, this alignment-and-adaptation operation needs to be energy efficient and computationally simple.

Although capacitive coupling is more sensitive to separation between the chips than inductive coupling, capacitive plates exhibit less crosstalk and can be made smaller and denser. Additionally, inductive proximity communication tends to have higher power consumption, since it requires either a constant current drive [7] or imposes tight timing requirements at the receiver to capture current pulse inputs [8]. Given the requirements for extremely low power and the ability to sense alignment, a capacitive solution has been used.

The proximity interconnect is formed by capacitive coupling between plates in the pad-level metal of the two chips (Fig. 1). Since only one side of the link needs to be able to sense alignment, two different array types, sensor and target, are used. The target array contains only a transmitter and receiver, while the sensor array adds alignment sensing blocks. Embedding both alignment sensing and communication operations in the same (sensor) array eliminates the need to infer link quality from a separate alignment sensor,

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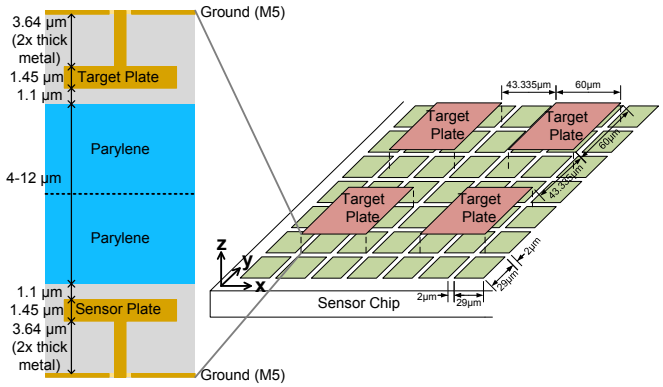

Fig. 1. Dielectric layers and sensor/target array arrangment (target chip outline not shown for clarity).

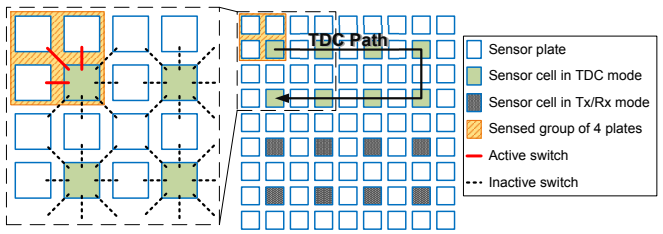

Fig. 2. Structure of the sensor array, showing TDC path for alignment sensing at indicated plates.

thus simplifying the alignment-and-adaptation operation. In order to increase granularity during alignment sensing and to maximize coupling capacitance for communication, the sensor array is composed of smaller plates that can be connected together in groups of four; each group of four sensor plates corresponds in size to a single target plate. The target plate pitch is $3^1/_3$ times the sensor plate pitch. Although this large spacing reduces signaling density, it minimizes crosstalk and avoids the need for differential crosstalk-mitigation schemes [6], allowing a lower-power single-ended design. Using a non-integer multiple of the sensor plate pitch prevents all the target plates from being simultaneously poorly aligned to the sensor, thus allowing the adaptation scheme some flexibility to optimize the array for a given data rate under different alignment conditions.

The dielectric between the two plates is composed of the passivation as well as a parylene sheet 4-12 μm thick, depending on the exact structure of the parylene module. Since the distance between the plates can be relatively large compared to the distance between each plate and its corresponding ground plane (Fig. 1), it is difficult to distinguish the capacitance between the sensor and the target plate from that between the sensor and the ground plane under the target plate. Instead, a stimulus (e.g. an alternating sequence) is applied to the target plate to electronically differentiate it from the ground plane. The amplitude received at the sensor is proportional to the amount of coupling between the plates, and this signal is rectified into a bias for a voltage-controlled delay line (VCDL). The output of the VCDL is in turn converted into a digital word via a time-to-digital converter (TDC).

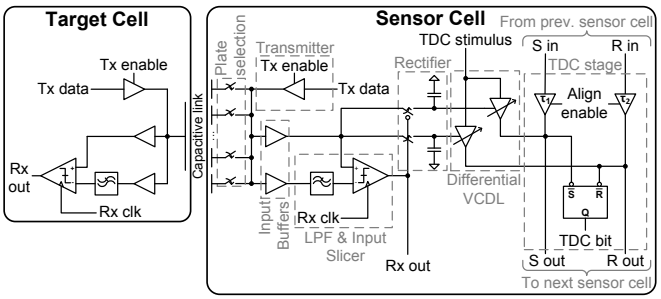

Fig. 3. Architecture of the sensor and target cells, with key functional blocks highlighted.

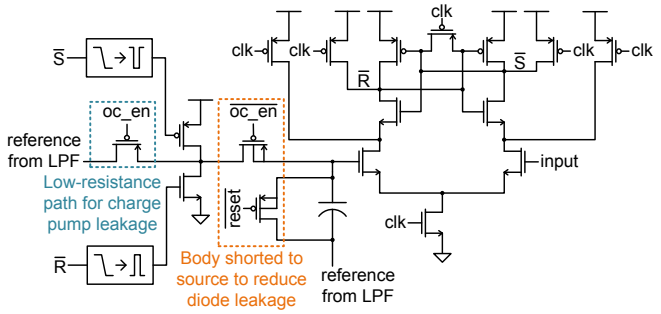

Fig. 4. Input slicer and offset compensation (SR latch not shown). 'Reset' zeroes the offset compensation capacitor, 'oc_en' is asserted during offset compensation calibration.

III. System Architecture

The structure of the sensor array is presented in Fig. 2. Each sensor cell can associate itself with one of 4 possible groups of 4 sensor plates, and shares these plates with its neighbours (the control logic ensures that no plate is connected to more than one cell at a time). In order to save power and area, the TDC stages are distributed through the sensor array, one stage per cell. During alignment sensing, 8 of these stages are connected to form a complete 3-bit TDC. By comparison, the structure of the target array is simple - each target plate is uniquely associated with a single target cell, which contains the transmitter and receiver for that plate

The architecture of the sensor and target array cells is presented in Fig. 3. Since the target cell is a subset of the sensor cell, subsequent discussion will focus on the design of the sensor cell.

Each sensor cell connects to one of 4 different groups of plates, so a set of switches is provided to select the correct group. Source-follower buffers are used to isolate the plates from the rest of the sensor cell blocks in order to minimize parasitic loading of the capacitive link. The transmitter is a simple tri-state buffer, modified with a leakage path to bias the source-follower buffers appropriately. These source follower buffers drive two distinct signal paths - the first contains no filtering, and is used by both the input slicer and the rectifier. The second path contains a low-pass filter, and is used to generate a reference voltage for the input slicer.

The input slicer itself is a strongARM latch used as a comparator (Fig. 4), followed by an SR latch. Chip-to-chip data rates in the 10's of Mbps are targeted, so latch gain is made fairly low in order to save power. Offset is a more

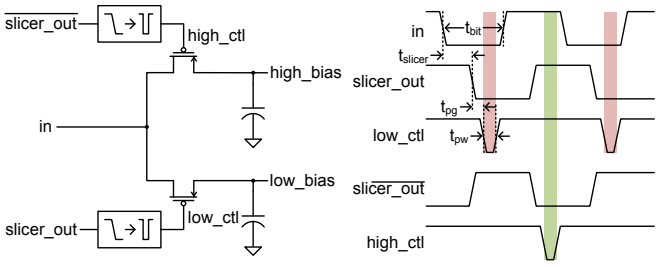

Fig. 5. Rectifier and associated timing diagram. To capture the correct value, $t_{slicer} + t_{pg} + t_{pw} < t_{bit}$.

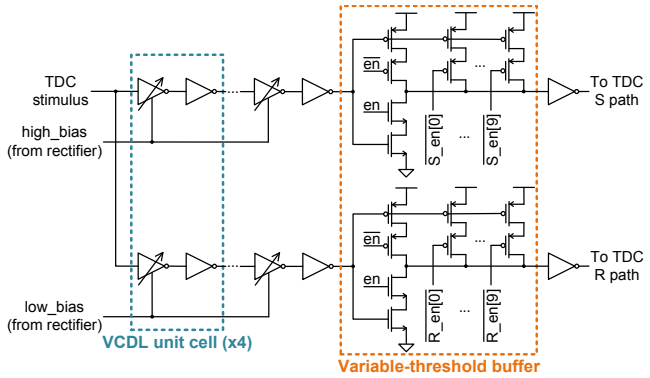

Fig. 6. Differential voltage-controlled delay line.

pressing concern, since the received signal amplitudes can be small if the alignment is poor. Monte Carlo simulation of the input slicer suggests that it has a 3-sigma offset of $\sim\pm$50 mV; in order to correct this to $<$10 mV within a limited power and area budget, charge pump-based offset compensation is added in series with the low-pass filter generating the reference voltage. Leakage is reduced through the use of a thick-oxide storage capacitor, triple-well devices to eliminate diode leakage through switches and the provision of a low-resistance path to shunt leakage from the charge-pump switches away from the storage capacitor. These measures limit charge pump leakage to about 1 mV/ms in the FF corner, and it can be refreshed periodically when the link is taken down to re-acquire chip-to-chip alignment.

The rectifier observes the input slicer output; when the output transitions, it generates pulses to control switches that shunt the high or low levels of the input signal onto the appropriate storage capacitor (Fig. 5). The delay from a transition in the input signal to the pulse must be short enough so that the pulse ends before a further transition in the input signal; to increase timing margin, the target cell transmitter is set to a low-frequency mode during alignment sensing.

The rectified voltages are used to bias a differential VCDL (Fig. 6). Offset error of the ADC formed by the VCDL and TDC is the most significant error affecting the assessment of link quality and alignment. This is corrected by a variable-threshold buffer at the output of VCDL, adjusted by observing the zeroth TDC output bit (prior to any TDC delay elements). The TDC is a straightforward vernier design. The differential delay is generated by adding a capacitive load to one signal path, so that $\tau_1 > \tau_2$. An SR-latch arbiter is used for symmetry.

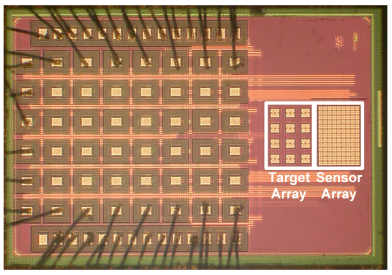

Fig. 7. Die micrograph, with sensor and target arrays marked.

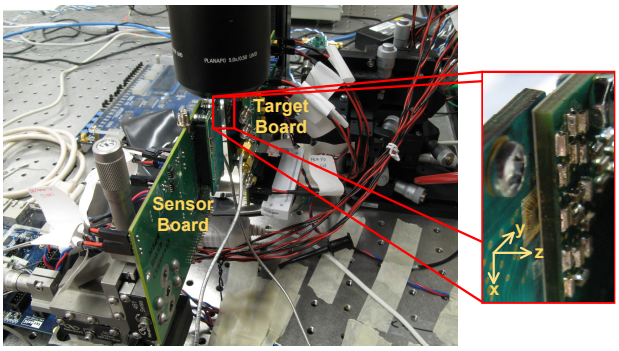

Fig. 8. Test setup. Inset: Detail of chips when brought into alignment.

IV. Measurement Results

Both a 6x4 cell (13x9 plate) sensor and a 4x3 cell target array were implemented in a single 65 nm bulk CMOS test chip (Fig. 7). The sensor plates measure 29x29 μm with 2 μm spacing, while the target plates are 60x60 μm. The sensor cell circuitry and digital logic for testing are designed to fit within a 2x2 set of sensor plates (62x62 μm). The target cell electronics are likewise designed to fit under a single target plate. Two test chips were mounted on a pair of micropositioners, and aligned visually under a microscope (Fig. 8). Slight over-torque was applied in order to cause the PCBs to flex against each other and ensure the test chips were reasonably close [5]. The alignment-sensing function of the sensor array was then used to correct any remaining alignment error. Tests were conducted with different thicknesses of parylene (4, 5, 6, 2x4, 2x5 and 2x6 μm, with $\pm$0.5 μm tolerance) by adhering a single sheet of parylene to the sensor chip and adding a second sheet to the target, as necessary.

The alignment sensing was tested at various thicknesses of parylene, both for vertical (Z-axis) separation (Fig. 9) and in-plane (X/Y-axis) misalignment (Fig. 10). Vertical separation is measured directly from the appropriate sensor cell's TDC output. Since the amount of coupling capacitance is inversely proportional to the distance between plates, achieved resolution depends on the amount of separation and parylene between the chips, and varies from 1-4 μm/LSB. In-plane misalignment can be estimated by taking the ratio of adjacent sensor cell outputs; just as with vertical separation measurements, resolution degrades as coupling gets smaller. An in-plane alignment resolution between 3-20 μm is achieved.

When properly aligned, communication over all 12 channels available was demonstrated at data rates up to 60 Mbps/channel with BER $< 10^{-9}$. Input slicer offset compen-

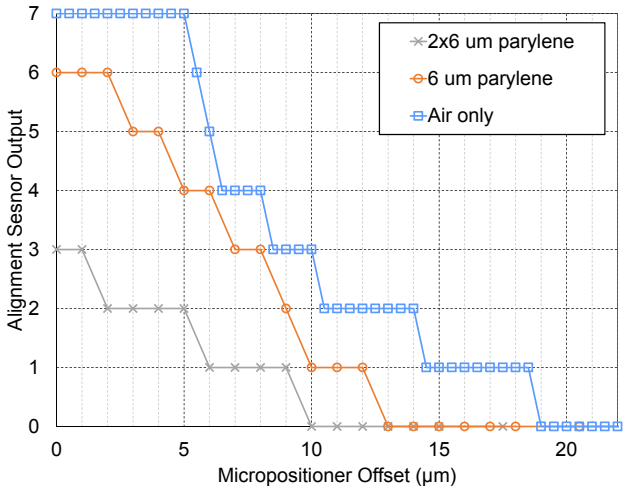

Fig. 9. Alignment sensor output under vertical (Z-axis) separation. Readings for micropositioner offsets <2 μm experience some non-linearity due to over-torquing of the two chips against each other. Coupling with air-only dielectric is good enough to cause the alignment sensor output to saturate.

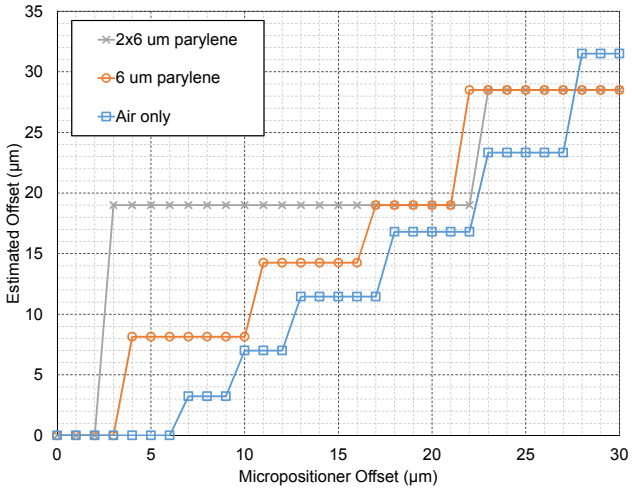

Fig. 10. Alignment sensor output under in-plane (X/Y-axis) misalignment. Resolution degrades substantially as parylene thickness is increased, due to the reduction in coupling between sensor and target plates.

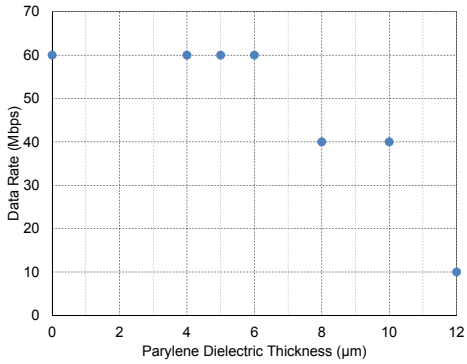

Fig. 11. Maximum data rates achievable (BER $< 10^{-9}$) under best-case alignment, for various thickness of parylene dielectric.

TABLE I
PERFORMANCE SUMMARY

Process	65 nm bulk CMOS
Die Area	1.6 mm x 2.4 mm
Sensor Array Area	401 μm x 277 μm
Target Array Area	370 μm x 267 μm
Data Rate	12 x 60 Mbps
Transmitter & Input Buffer Supply	1.0 V
Slicer, Rectifier, VCDL & TDC Supply	0.7 V
Power Dissipation (Sensor + Target)	
Transceiver @ 12 x 60 Mbps	100.9 μW + 27.7 μW
Alignment Sensor	23.1 μW + 20.2 μW
Figures-of-Merit	
Power	0.180 pJ/bit
Area (based on sensor array size)	6446 Mbps/mm^2

sation was run for $\sim$10 μs (600 clock cycles @ 60 Mbps) every 2 ms, for a net data rate (over 12 channels) of $\sim$716 Mbps. Total power consumption at this data rate was 129 μW (Table I). Maximum achievable data rate is dependent on the amount of coupling between target and sensor plates; this is presented against parylene thickness in Fig. 11.

V. CONCLUSION

A capacitive proximity interconnect for Origami biomedical implants has been developed and fabricated in 65 nm CMOS. The array embeds a distributed TDC-based chip-to-chip alignment sensor that provides direct information about link quality, enabling straightforward adaptation of the link to changing alignment conditions. Communication through up to 12 μm of parylene-C has been demonstrated with data rates from 10-60 Mbps and power efficiency of 0.180 pJ/bit.

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