A Low-power 20Gb/s Transmitter in 65nm CMOS Technology

Meisam Honarvar Nazari, Azita Emami-Neyestanak

California Institute of Technology, Pasadena, California, 91125, USA

***Abstract*- A 20Gb/s transmitter employing an analog filtering pre-emphasis equalization technique is presented. The transmitter dissipates 10mW from a 1.2V supply and occupies 0.01mm^2. This high-frequency boosting equalization technique allows for compensating channel losses up to 20dB at Nyquist-rate. The prototype was fabricated in 65nm CMOS technology and characterized using lossy cables and 5" and 10" FR4 PCB traces.**

***Index terms* — Transmitter, equalization, intersymbol interference (ISI), pre-emphasis.**

I. INTRODUCTION

One of the main challenges of the modern wireline communication systems is the severe frequency-dependent loss in the channel. Even a relatively short channel can introduce large distortions at high data rates. The intersymbol interference (ISI) caused by the channel degrades the timing jitter, signal to noise ratio (SNR) and ultimately the bit error rate (BER). To compensate for channel losses, transmitter pre-emphasis, receiver equalization or both can be applied. Receiver equalization typically involves mixed-signal circuitry with stringent speed, accuracy and noise requirements. This leads to considerable power overhead. Low-power equalization at the transmitter can simplify the design of the receiver and help with the overall power consumption [1].

Finite impulse response (FIR) and analog filters are the two most commonly used techniques for transmitter pre-emphasis [2]-[5]. FIR-based transmitters require additional hardware for generating delayed versions of the data. At high data rates the extra hardware consumes a considerable amount of power. Additionally, FIR pre-emphasis reduces the output signal swing due to the low frequency attenuation of the transmitted data. As a result, the power penalty of employing this technique at high data rates can be very large. On the other hand, analog filtering does not require any additional active component and solely relies on passive devices and offers high power efficiency. Although passive devices occupy a large area, as the frequency of operation increases, the area drops. In addition, since high quality factor is not necessary, a 3D layout can help to reduce the area. The basic idea behind analog filtering technique is to boost the high frequency content of the transmitted signal to compensate the high frequency attenuation of the channel. In this paper we discuss a novel transmitter employing analog filtering that enables data rates up to 20Gb/s over high loss channels.

II. SYSTEM ARCHITECTURE

Shunt, series, shunt-series, and shunt-double-series techniques have been previously used in order to enhance the bandwidth of amplifiers and compensate capacitive loads [6]. In many signaling applications, the bandwidth of the links is limited due to the lossy-capacitive (RC) behavior of the channel. In this work, modified peaking techniques are employed to compensate the effective capacitance of the trace and equalize the channel loss. The maximum bandwidth enhancement can be achieved through employing the shunt and double-series technique, which involves using six inductors in a differential implementation as shown in Fig. 1.

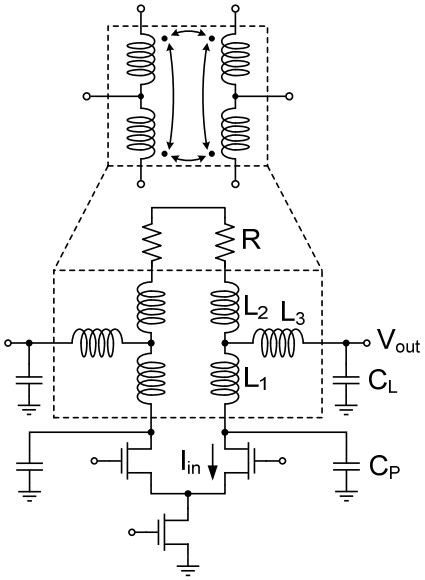


Fig. 1. Shunt and double-series bandwidth enhancement technique.

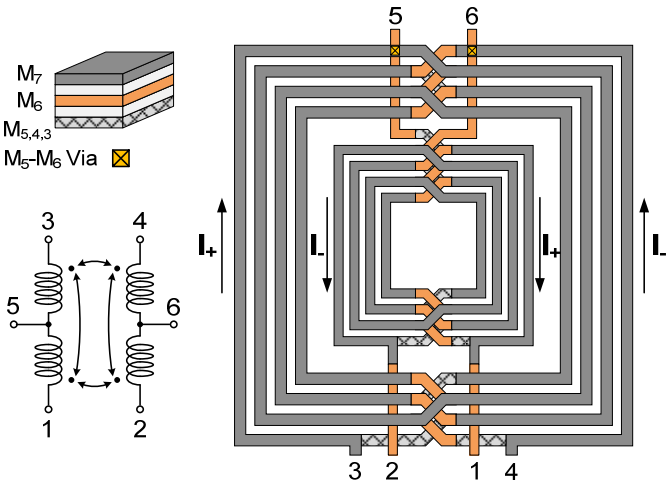
In this technique the line capacitance (C_L) forms a series LC with L_3. As a result, the effect of C_L is cancelled at the resonant frequency $1/(2\pi\sqrt{L_3C_L})$. Around this frequency, the transfer function from the differential pair transistor current (I_{in}) to the output can be simplified to equation (1). L_1 and C_P form a pair of complex conjugate poles that introduce a considerable amount of peaking in the transfer function.

$$\left|\frac{V_{out}}{I_{in}}\right| = \frac{1}{(1-L_1C_P\omega^2)\times C_L\omega} \quad (1)$$

As the quality factor of the inductor is not high, a fairly broadband peaking is obtained. Another zero at $f_z=R/(2\pi L_2)$ can be added to the transfer function through L_2, as in shunt peaking technique. The main drawback of this technique is the excessive silicon area required. In order to alleviate the area penalty, the inductors are replaced by two T-coils [6] that offer the same performance as shown in Fig. 1. To further improve

the area efficiency of this technique, we have utilized the fact that the two branches of the differential transmitter carry currents in opposite directions. By mutually coupling the coils in two branches, we obtain the same inductance in a smaller area.

$$L_{eff} = L + M \quad (2)$$



L_1	500pH	C_3	10fF
L_2	540pH	M_1	200pH
R_1	6.5Ω	M_2	350pH
R_2	6.4Ω	M_3	210pH
C_1	10fF	M_4	240pH
C_2	10fF		

L_1	230pH	C_3	5fF
L_2	190pH	M_1	55pH
R_1	4.0Ω	M_2	105pH
R_2	4.2Ω	M_3	64pH
C_1	5fF	M_4	82pH
C_2	5fF		

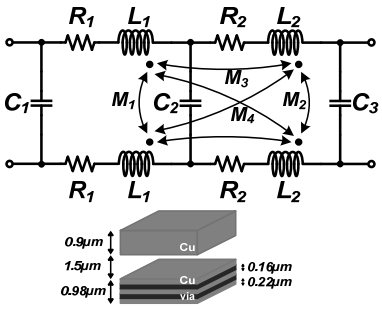
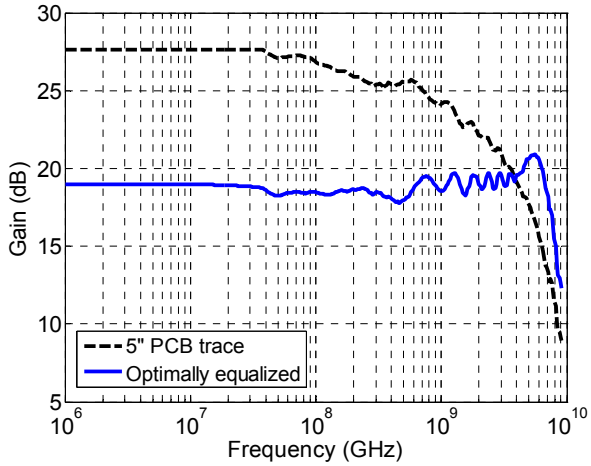
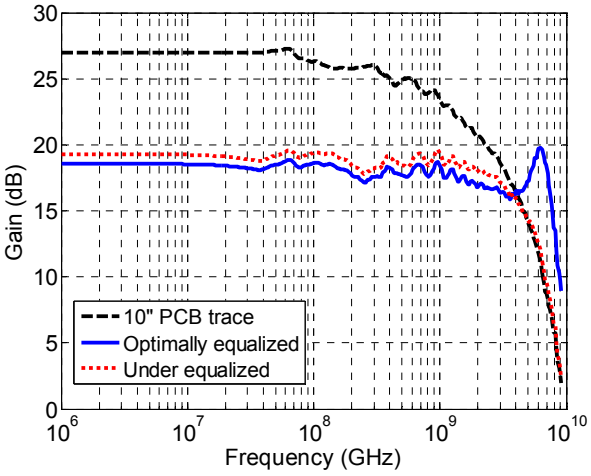


Fig. 2. Segmented T-coil layout and model generated using IE3D electromagnetic simulator.

Moreover, the opposite direction currents in the two branches significantly reduce the magnetic field outside the T-coil area, allowing for dense arrays of transmitters without considerable crosstalk between them. Fig. 2 shows the schematic and layout of the coupled T-coils. They are interwound using three thick metal layers. Although the utilized technology provides only two thick metal layers, a third is realized by stacking three thin metal layers as shown in Fig. 2. In order to be able to equalize different channels with different amount of loss, the inductors in each T-coil are segmented using MOS switches with 2 bits of resolution (Fig. 4). This allows for adjusting the inductance to introduce different levels of peaking. In addition to inductive peaking, a zero-peaking technique is employed by adding a variable parallel RC to the source of the transmitter (Fig. 4). This introduces a zero at frequency $1/(2\pi RC)$. The variable resistor is implemented using an NMOS transistor in triode. According to simulation, about 10dB of peaking is achieved by using this technique. The transmitter is comprised of two stages as shown in Fig. 4. The first stage is the pre-amplifier that drives the output stage. The output stage utilizes T-coil and zero peaking. The segmented T-coils were simulated in an electromagnetic simulator (IE3D) and modeled, shown in Fig. 2. Fig. 3(a), (b) show the simulation results for the transmitter connected to two different channels. The channel response, along with different levels of pre-emphasis, is shown for 5" and 10" FR4 PCB traces. An improvement in bandwidth from 800MHz to 8GHz is achieved with optimal pre-emphasis.



(a)



(b)

Fig. 3. Simulated transfer characteristics of the transmitter and channel for different levels of pre-emphasis, (a) 5" FR4 channel, (b) 10" FR4 channel.

III. MEASUREMENT RESULTS

The prototype was fabricated in a 65nm CMOS process. The chip micrograph is shown in Fig. 9. The transmitter consumes 10mW from a 1.2V supply and provides 250mV (peak-to-peak) output swing. The transmitter was tested with an on-chip PRBS-7 generator. A high speed, 32bit shift register was also integrated to enable applying arbitrary patterns to the transmitter for testing and debugging purposes. The output of

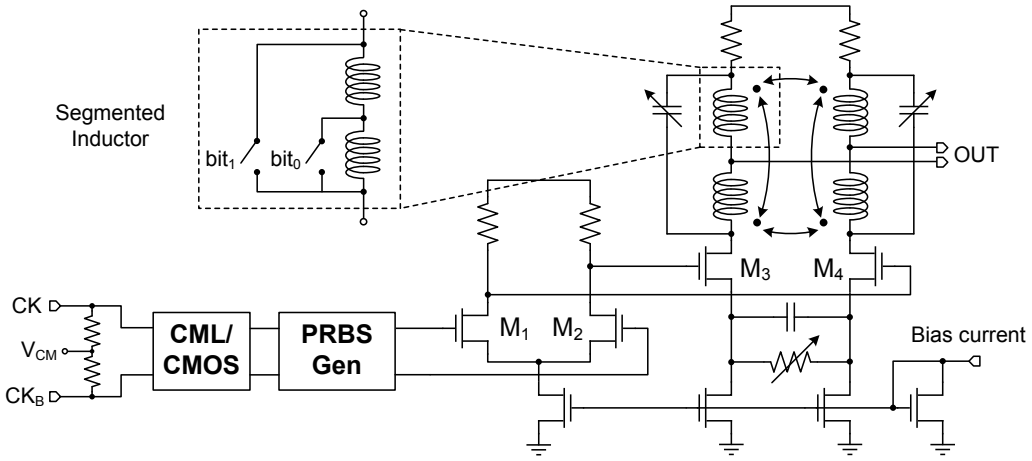


Fig. 4. Transistor-level schematic of the transmitter employing segmented T-coils.

the on-chip PRBS-7 generator was sent through a lossy cable as well as 5" and 10" FR4 PCB traces at maximum rate of 20Gb/s. Fig. 5 shows the transfer characteristics of these channels. A 2-tap FIR was simulated in MATLAB with the same channels to compare the performance of the analog filter and FIR-based pre-emphasis techniques in channel loss compensation. As shown in Fig. 6, by employing the proposed pre-emphasis technique at 15 Gbps over the lossy cable (7dB loss at 7.5GHz), a completely open eye with less than 12ps peak-to-peak jitter was measured. Fig. 7 illustrates the measured and simulated eye-diagrams at the output of 5" and 10" FR4 channels while a 15Gb/s data was sent by the proposed transmitter and a 2-tap FIR respectively. The 5" and 10" FR4 channels introduce about 15dB and 20dB loss at 7.5GHz. A 20Gb/s data was also sent through the lossy cable with 10dB loss at 10GHz. The output eye-diagram has less than 18ps peak-to-peak jitter as shown in Fig. 8. It is important to note that the circuit non-idealities are not included in the simulations of the 2-tap FIR and the actual circuit performance is expected to be worse.

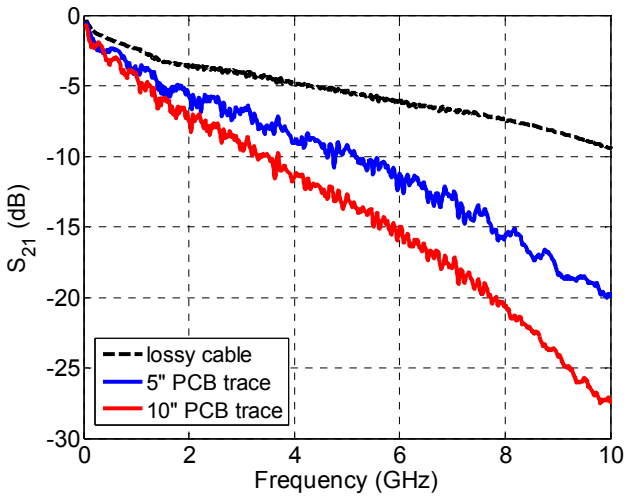


Fig. 5. Channels transfer characteristics.

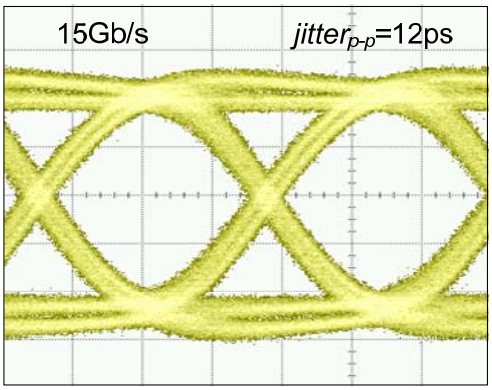


Fig. 6. Transmitter output at 15Gb/s over lossy channel with 7dB loss.

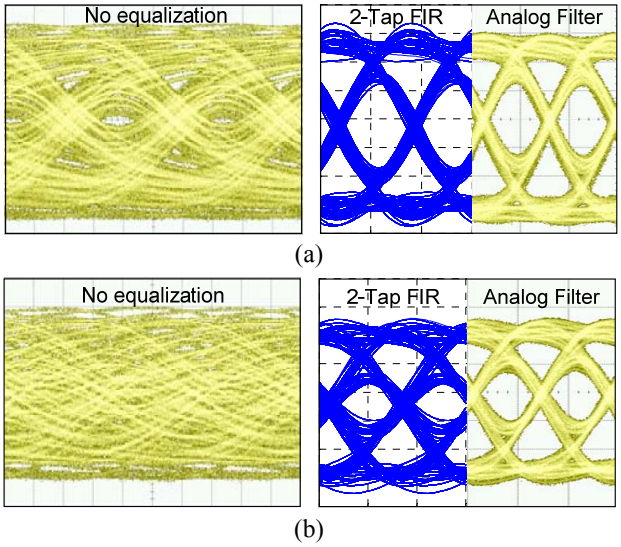
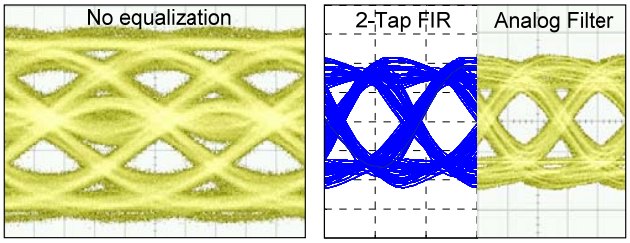


Fig. 7. Output of the channel before and after equalization with the 2-tap FIR equalizer and analog filter. (a) at 15Gb/s over 5" FR4, (b) at 15Gb/s over 10" FR4.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER DESIGNS.

	This work	[2]	[3]	[4]	[5]
Rate	20Gb/s	20Gb/s	10.3Gb/s	20Gb/s	40Gb/s
Loss	**20dB**	12.8dB	18dB	10dB	19dB
power	**10mW**	59mW	0.26W*	45mW	135mW
TX output	250mVpp	300mV	250mV	400mV	-
Process	65nm	65nm	90nm	65nm	65nm
Supply	1.2V	1.2V	1.2V	1.2V	1.2V
Area	**0.01mm^2**	0.29mm^2	0.166mm^2	0.03mm^2	0.63mm^2
Type	Analog Filter	2-Tap FIR	3-Tap FIR	2-Tap FIR	5-Tap FIR

* Includes the entire transceiver



(a) (b)

Fig. 8. 20Gb/s output over lossy channel with about 10dB loss at Nyquist rate, (a) before equalization, (b) after equalization with 2-tap FIR (left, simulated) and analog filter (right, measured).

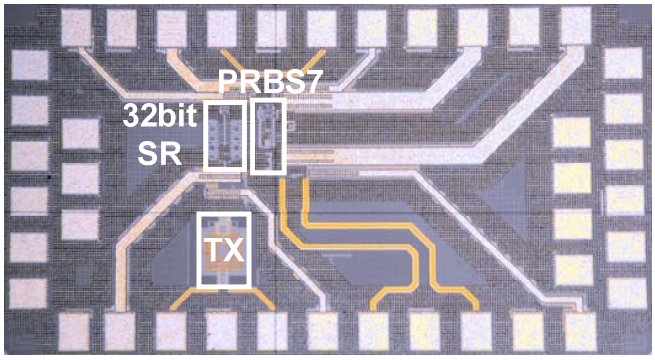


Fig. 9. Transmitter die micrograph.

The high frequency peaking introduced in this technique may cause extra far-end crosstalk (FEXT) in highly parallel communication links. The resulting crosstalk can be cancelled employing low-power crosstalk cancellation techniques [7].

Table I compares the performance of this design with FIR-based transmitters. To achieve the same output swing, the 2-tap FIR requires twice as much power as the proposed design. In many FIR-based pre-emphasis designs [2-5] shunt peaking inductors are required to meet the bandwidth constraint of the CML delay elements. These inductors impose a large area penalty as shown in table I. The comparison table and the measured/simulation results in Fig. 7 and Fig. 8 show superior performance for the analog filter-based equalization technique both in terms of channel loss compensation and power and area efficiencies.

IV. CONCLUSION

A 20Gb/s transmitter utilizing efficient analog filtering is presented. The proposed pre-emphasis technique supports data transmission over PCB channels with loss levels in excess of 20dB at BER<10^{-12}. The proposed architecture consumes significantly less power compared to an FIR transmitter that has similar performance, while occupying very small silicon area.

ACKNOWLEDGMENTS

The authors acknowledge the support of NSF and Intel as well as STMicroelectronics for fabricating the chip. M. Nazari would like to thank Z. Safarian for constant help and support.

REFERENCES

[1] J. H. R. Schrader, E. A. M. Klumperink, J. L. Visschers, B. Nauta, "Wireline Equalization using Pulse-Width Modulation", *IEEE Custom Integrated Circuits Conf.*, pp. 591-598, Sept. 2006

[2] S. Y. Kao, S. I. Liu, "A 20-Gb/s Transmitter with Adaptive Pre-emphasis in 65-nm CMOS Technology", *IEEE Trans. on Circuits and Systems*-II, Vol. 57, No. 5, May 2010

[3] Y. Hidaka, et al., "A 4-Channel 1.25–10.3 Gb/s Backplane Transceiver Macro With 35 dB Equalizer and Sign-Based Zero-Forcing Adaptive Control", *IEEE Journal of Solid State Circuits*, Vol. 44, No. 12, Dec 2009

[4] H. Wan, J. Lee, "A 21-Gb/s 87-mW Transceiver With FFE/DFE/ Analog Equalizer in 65-nm CMOS Technology", *IEEE Journal of Solid State Circuits*, Vol. 45, No. 4, April 2010

[5] M. S. Chen, Y. N. Shih, C. L. Lin, H. W. Hung, J. Lee, "A 40Gb/s TX and RX Chip Set in 65nm CMOS", *Int. Solid State Circuit Conf.* (ISSCC), pp. 146-147, Feb. 2011

[6] T. H. Lee**,** "The Design of CMOS Radio-Frequency Integrated Circuits"**,** 2nd edition, Cambridge University Press, 2003

[7] M. Honarvar Nazari, A. Emami-Neyestanak, "A 15Gb/s 0.5mW/ Gb/s 2-Tap DFE Receiver with Far-End Crosstalk Cancellation", *Int. Solid State Circuit Conf.* (ISSCC), pp. 146-147, Feb. 2011

[8] J. Kim, et al., "Circuit Techniques for a 40Gb/s Transmitter in 0.13µm CMOS", *Int. Solid State Circuit Conf.* (ISSCC), pp. 150-151, Feb. 2005

[9] Z. Safarian, H. Hashemi, "A 1.3–6 GHz triple-mode CMOS VCO using coupled inductors" *IEEE Custom Integrated Circuits Conf.*, pp. 69-72, Sept. 2008