

# A 24-Gb/s Double-Sampling Receiver for Ultra-Low-Power Optical Communication

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**Abstract**—This paper describes a dense, high-speed, and low-power CMOS optical receiver implemented in a 65-nm CMOS technology. High data rate is achieved using an *RC* double-sampling front-end and a novel dynamic offset-modulation technique. The low-voltage double-sampling technique provides high power efficiency by avoiding linear high-gain elements conventionally employed in transimpedance-amplifier (TIA) receivers. In addition, the demultiplexed output of the receiver helps save power in the following digital blocks. The receiver functionality was validated by electrical and optical measurements. The receiver achieves up to 24 Gb/s data rate with better than 160- $\mu$ A current sensitivity in an experiment performed by a photodiode current emulator embedded on-chip. Optical measurements performed by a 1550-nm wire-bonded photodiode show better than  $-4.7$ -dBm optical sensitivity at 24 Gb/s. The receiver offers peak power efficiency of 0.36 pJ/b at 20 Gb/s from a 1.2-V supply and occupies less than 0.0028 mm<sup>2</sup> silicon area.

**Index Terms**—Demultiplexing, double-sampling, dynamic offset modulation, low-power, optical interconnects, optical receiver.

## I. INTRODUCTION

INTEGRATED circuit scaling has enabled a huge growth in processing capability, which necessitates a corresponding increase in inter-chip communication bandwidth. This trend is expected to continue, requiring both an increase in the per-pin data rate and the I/O number. Unfortunately, the bandwidth of the electrical channels and the number of pins per chip do not follow the same trend. As data rates scale to meet increasing bandwidth requirements, the shortcomings of copper channels are becoming more severe. While I/O circuit performance favors from technology scaling, the bandwidth of electrical channels does not scale with the same trend. In particular, as data rate increases, they pose excessive frequency-dependent loss, which results in significant intersymbol interference (ISI). In order to continue scaling data rates, equalization techniques can be employed to compensate for the ISI [1]–[3]. However, the power and area overhead associated with equalization make it difficult to achieve target bandwidth with a realistic power budget. As a result, rather than being technology-limited, current high-speed I/O link designs are becoming channel- and power-limited.

A promising solution to the I/O bandwidth problem is the use of optical interchip communication links. The negligible frequency-dependent loss of optical channels provides the potential for optical link designs to fully utilize increased data rates provided through CMOS technology scaling without excessive equalization complexity. Optics also allows very high information density through wavelength-division multiplexing (WDM). Hybrid integration of optical devices with electronics has been demonstrated to achieve high performance [4]–[9], and recent advances in silicon photonics have led to fully integrated optical signaling [10], [11]. These approaches pave the way to massively parallel optical communications. In order for optical interconnects to become viable alternatives to established electrical links, they must be low-cost and have competitive energy- and area-efficiency metrics. Dense arrays of optical detectors require very low-power, sensitive, and compact optical receiver circuits. Existing designs for the input receiver, such as TIA, require large power consumption to achieve high bandwidth and low noise and can occupy large area due to bandwidth enhancement inductors. Moreover, these analog circuits require extensive engineer efforts to migrate and scale to future technologies.

In this work, a compact low-power optical receiver that scales well with technology has been designed to explore the potential of optical signaling for future chip-to-chip and on-chip communication. This paper is organized as follows. In Section II, we present the overall architecture of the receiver. We introduce the existing techniques employed in optical receivers such as TIA [4]–[8] and integrating double-sampling [9], [15] and discuss their challenges. Next, we will present the proposed solution to these challenges, which is an *RC* double-sampling front-end. In Section III, we present the detailed circuit-level implementation of the proposed receiver along with the sensitivity analysis. System-level design considerations such as clocking and adaptation for the proposed receiver are discussed in Section IV. In Section V, we present experimental results from the evaluation of a 65-nm bulk CMOS implementation of the optical receiver. Finally, Section V summarizes the work with a comparison to prior works.

## II. RECEIVER ARCHITECTURE

The task of the optical receiver is to resolve the value of the incoming signal by sensing the changes in the magnitude of photodiode current. To minimize the transmit optical power, the receiver has to be able to resolve small optically generated current from the photodiode. In order to achieve a robust data resolution with low BER, the total input-referred noise current from the circuitry and the diode itself should be well below the optically generated current. In general, design of a low-noise

Manuscript received June 20, 2012; revised August 28, 2012; accepted October 24, 2012. Date of publication December 20, 2012; date of current version January 24, 2013. This paper was approved by Associate Editor Anthony Chan Carusone.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2012.2227612

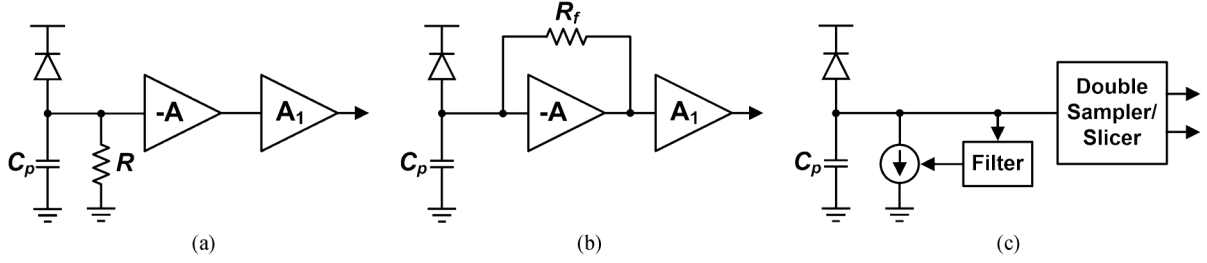


Fig. 1. Different optical receiver architectures. (a) Simple resistive front-end. (b) Transimpedance front-end with limiting amplifiers. (c) Integrating double-sampling receiver.

front-end with a very high bandwidth is difficult and requires high electrical power consumption. In most optical receivers, the photodiode current is converted to a voltage signal. A simple resistor, shown in Fig. 1(a), can perform the  $I$ - $V$  conversion if the resulting  $RC$  time constant is on the order of the bit interval ( $T_b$ ) [10]. A voltage amplifier then amplifies the voltage swing for the following data-resolution slicer block. Assuming that the voltage amplifier has a high bandwidth, the bit rate of such a front-end is limited by the input node time constant  $RC_{in}$ , where  $C_{in}$  is the sum of diode capacitance and other parasitic capacitors at the input node. The time constant of the input node sets a maximum limit on the resistor  $R$ . On the other hand, the maximum possible voltage swing at this node is equal to  $\Delta V = RI_{op}$  where  $I_{op}$  is the input photocurrent. It is clear that lower  $R$  values degrade the signal-to-noise-ratio (SNR) at the input. This results in a strong tradeoff between the sensitivity and the bandwidth as they both depend on  $R$ . This tradeoff between sensitivity and data rate can be resolved by employing TIAs [see Fig. 1(b)]. TIA provides low impedance at the input node while introducing a high transconductance to convert the optical current from the photodiode into voltage. As shown in

$$BW = \frac{1 + A}{2\pi R_f C_{in}} \quad (1)$$

the maximum bandwidth, and hence the data rate, supported by TIA is proportional to its gain  $A$ .

As a result, to achieve a high data-rate, a TIA with large gain-bandwidth product is required, which can result in high power consumption. Passive components such as inductors can be employed to enhance the bandwidth of TIA [4]–[6], but impose a significant area overhead. As an example, an inverter can be employed as the gain stage in the TIA, as shown in Fig. 2(a). The resulting input resistance  $R_{in}$  and transimpedance  $R_t$  can be expressed as

$$R_{in} = \frac{R_F + r_{ds}}{1 + g_m r_{ds}} \quad (2)$$

$$R_t = \frac{g_m R_F - 1}{1 + g_m r_{ds}} r_{ds}. \quad (3)$$

Fig. 2(b) shows how data rate changes with  $R_t$  for different photodiode parasitic capacitance in 65-nm CMOS process. It can be seen that, for  $C_{in} = 200$  fF, it is not possible to achieve 20 Gb/s operation. Fig. 2(c) shows the power consumption of this design. It should be noted that to achieve high sensitivity larger transimpedance is required. As a result, additional gain stages are required to enable high sensitivity, which adds to the

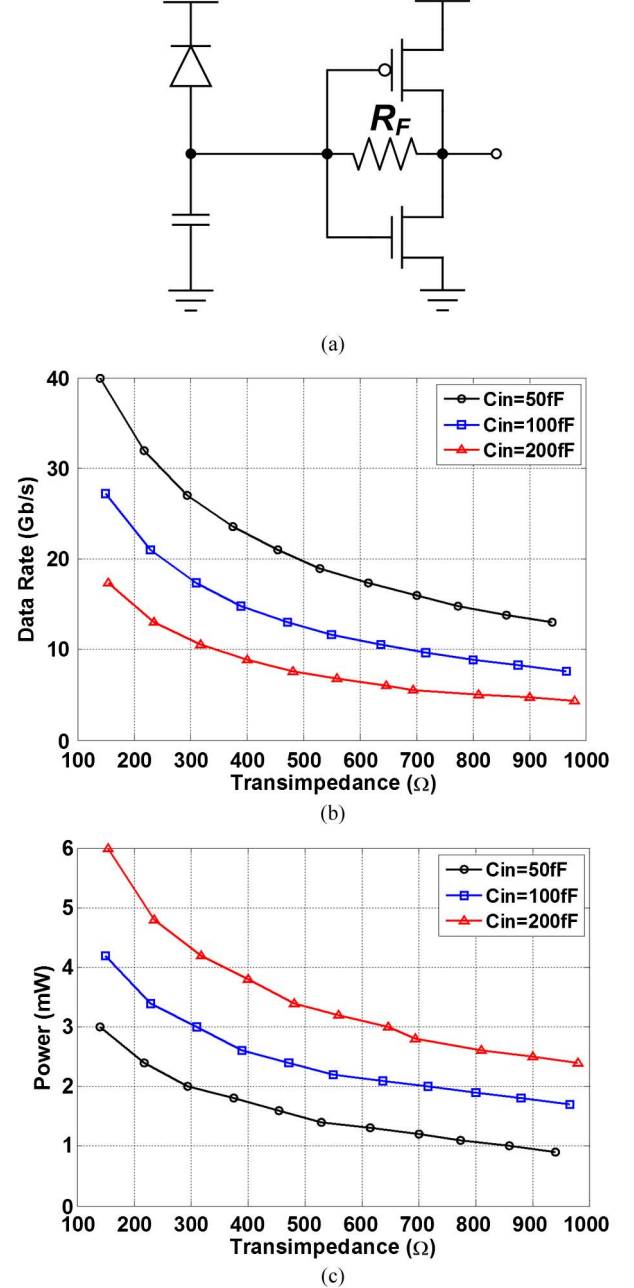


Fig. 2. (a) Inverter-based TIA. (b) TIA data rate. (c) Power consumption versus transimpedance for different photodiode capacitances.

overall power consumption. To achieve high data rates, TIA architectures such as [6] can be employed, however, the additional

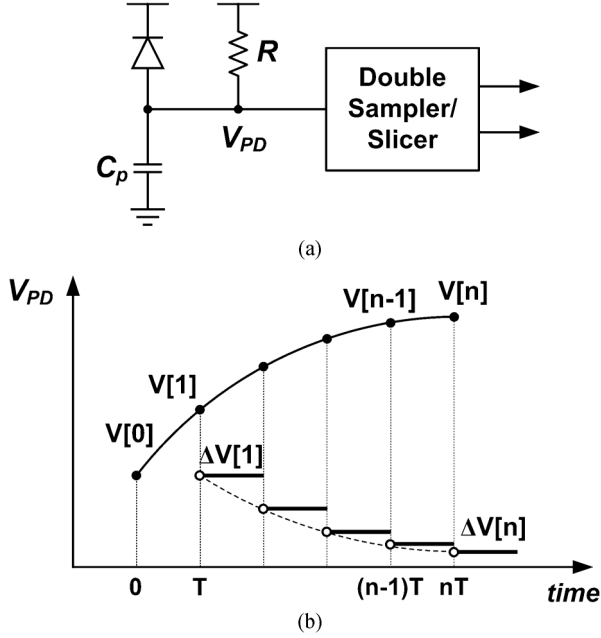


Fig. 3. (a) Proposed RC double-sampling front-end architecture. (b) Exponential input voltage and the corresponding double-sampled voltage for a long sequence of successive "1."

power and area is significant. High power consumption and area requirement as well as poor scalability make TIA design challenging for future highly parallel optical links.

An alternative to TIA is the integrating front-end [15], shown in Fig. 1(c). The input signal from the photodetector is a single-ended, positive current. The injected charge is higher if the bit value is "1," but it is not necessarily zero when the bit value is "0." Therefore, in order to have a bipolar voltage change at the input of receiver a constant charge is subtracted from the input capacitor for every bit. This is done by subtracting an adjustable current from the input through a feedback loop. By sampling the input voltage at the end of each bit period the received bit is resolved. The double-sampling technique allows for immediate demultiplexing at the front-end by employing multiple clock phases and samplers. It also eliminates the need for high gain stages, such as TIA, that operate at the input data rate. Another advantage associated with this technique is the inherent single-ended to differential conversion that happens at the front-end and reduces receiver sensitivity to common-mode interferences. The main advantage of this technique is that it mainly employs digital circuitry that allows for achieving considerable power saving by scaling to advance technology nodes. However, this technique suffers from voltage headroom limitations and requires short-length dc-balanced inputs such as 8B/10B encoded data [9]. In this work, we propose an RC front-end that employs double sampling technique to break the trade-off between data rate and sensitivity without the described headroom problem, as shown in Fig. 3(a). This technique allows for an input time constant that is much larger than  $T_b$  ( $RC_{in} \gg T_b$ ) as opposed to TIA, in which the input time constant should be smaller than the bit time. The additional resistor  $R$  in the front-end automatically limits the input voltage and prevents out of range input

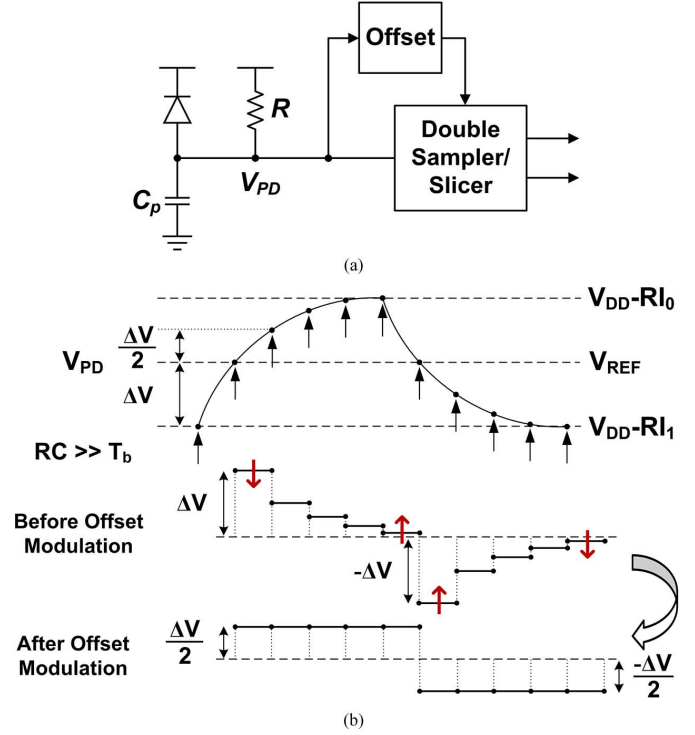


Fig. 4. (a) Modified RC front-end with DOM to resolve input dependent double-sampled voltage. (b) Basic operation of the DOM technique.

voltages due to long sequences of "1" or "0." The input voltage can be expressed as

$$V_{PD} = V_{DD} - RI_1 e^{\frac{-t}{RC_{in}}} \quad (4)$$

for a long sequence of "0" following a long sequence of "1," where  $V_{PD}$  denotes the input voltage,  $R$  is the front-end resistance,  $C_{in}$  is the total capacitance at the input, and  $I_1$  is the current due to a "1" input. Double-sampling can be applied to sample the input voltage at the end of two consecutive bit times  $V_{n-1}$  and  $V_n$  [see Fig. 3(b)] and these samples are compared to resolve each bit ( $\Delta V[n] = V_n - V_{n-1} > 0$  results in "1" and  $\Delta V[n] < 0$  results in "0"). However, the resistor causes the double-sampled voltage  $\Delta V[n]$  to be input-dependent as

$$V[n] = RI_1 e^{\frac{-nT_b}{RC_{in}}} \quad (5)$$

$$\Delta V[n] = RI_1 \left( 1 - e^{\frac{-T_b}{RC_{in}}} \right) e^{\frac{-(n-1)T_b}{RC_{in}}} = \Delta V[1] e^{\frac{-(n-1)T_b}{RC_{in}}} \quad (6)$$

where  $T_b$  denotes the bit time. For instance, a "1" after a long sequence of "0" generates larger  $\Delta V[n]$  than a "1" after a long sequence of "1." The dependency of the voltage difference on the input signal can be resolved by introducing a *dynamic offset* to the sense amplifier [see Fig. 4(a)]. This offset effectively increases the voltage difference  $\Delta V[n]$  for weak ones/zeros and decreases it for strong ones/zeros, as shown in Fig. 4(b). We call this technique dynamic offset modulation (DOM). The idea behind this technique is to introduce an offset to the double-sampled voltage based on the value of the voltage at the input. As an example, a long sequence of ones, followed by a long sequence of zeros is considered, Fig. 4(b). The first one after zeros generates a large voltage at  $V_{PD}$ . As the number of successive ones

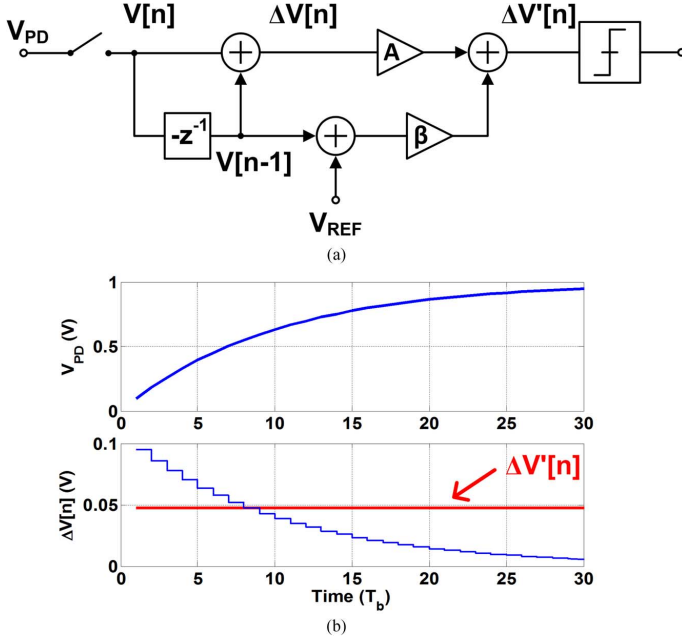


Fig. 5. (a) Block diagram of the offset modulation technique. The first sample is subtracted from the double-sampled voltage  $\Delta V[n]$  to make it constant regardless of the input sequence. (b) Simulated operation of the DOM for a long sequence of “1” showing  $\Delta V[n]$  before and after DOM.

increases, this voltage decays exponentially due to  $R$  and  $C_{in}$ . If the maximum double-sampled voltage is equal to  $\Delta V_{max}$ , DOM introduces an offset so that the sense amplifier differential input is  $\Delta V_{max}/2$ , regardless of the previous bits. For instance, an offset equal to  $-\Delta V_{max}/2$  is applied when  $\Delta V[n] = \Delta V_{max}$ , no offset is applied when  $\Delta V[n] = \Delta V_{max}/2$ , and an offset equal to  $\Delta V_{max}/2$  is applied if  $\Delta V[n] = 0$ .

Fig. 5(a) shows a simple model of the double sampler where  $\Delta V[n]$  can be expressed in the  $z$ -domain as

$$\Delta V(z) = (1 - z^{-1})V(z). \quad (7)$$

After subtracting the previous sample,  $V[n-1]$ , the resulting voltage difference  $\Delta V'[n]$  can be written in the  $z$ -domain as

$$\Delta V'(z) = (1 - z^{-1})V(z) + \beta z^{-1}V(z) \quad (8)$$

where  $\beta$  is the DOM coefficient and  $V(z)$  is equal to

$$V(z) = \frac{RI_1}{1 - e^{\frac{-T_b}{RC_{in}}} z^{-1}}. \quad (9)$$

In order to have a constant  $\Delta V'[n]$  regardless of the received input sequence, we should find  $\beta$  for which  $\Delta V'(z)$  is independent of  $z$ . By substituting (9) in (8), it can be shown that for

$$\beta = 1 - e^{\frac{-T_b}{RC_{in}}} \quad (10)$$

$\Delta V'(z)$  will be independent of  $z$  and equal to

$$\Delta V'[n] = \frac{1}{2} \Delta V_{max} \quad \forall n \quad (11)$$

where

$$\Delta V_{max} = RI_1 \left( 1 - e^{\frac{-T_b}{RC_{in}}} \right). \quad (12)$$

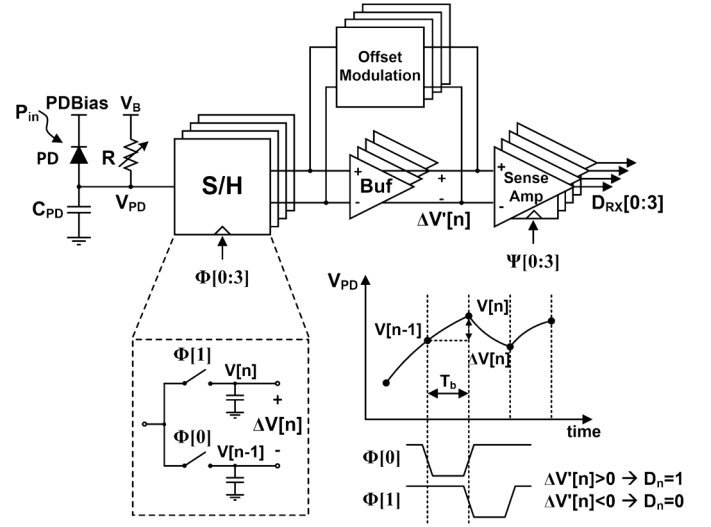


Fig. 6. Top level architecture of the RC double-sampling front-end.

$\Delta V_{max}$  is the double-sampled voltage due to a one (zero) following a long sequence of zeros (ones). Fig. 5(b) shows the simulation results showing the double-sampled voltage before and after DOM. The target value of  $\beta$  can be determined using adaptive algorithms as described in Section IV.

### III. ANALYSIS AND IMPLEMENTATION

Fig. 6 shows the top-level architecture of the receiver. The input current from the photodiode is integrated over the parasitic capacitor, while the shunt resistor ( $R$ ) limits the voltage.  $R$  can be designed to be adjustable to prevent saturation at high optical powers, allowing for a wide range of input optical power. As mentioned earlier, the employed double-sampling technique allows demultiplexing by use of multiple clock phases and samplers. In this design, a demultiplexing factor of four is chosen as the minimum possible demux factor to allow for proper operation of the double sampler and the following comparator stage. The front-end S/H is comprised of a PMOS switch and the parasitic capacitor ( $C_S$ ) from the following stage. The optimum size of  $C_S$  is chosen considering the noise performance of the front-end and S/H speed as will be explained later. An amplifier with about 6 dB of gain is inserted between the S/H and the comparator to provide isolation between the sensitive sampling node and the comparator and minimize kickback noise. This also creates a constant common-mode voltage at the comparator input and improves its speed and offset performance. A StrongARM sense amplifier [12] is employed to achieve high sampling rate and low power. Fig. 7 shows the transistor-level schematic of the sense amplifier. Banks of digitally adjustable NMOS capacitors are employed to compensate the offset due to mismatch. DOM is implemented using a differential pair at the input of the sense amplifier [13]. This differential pair along with the resistors of the buffer stage form an amplifier with variable gain  $\beta$ , which is adjusted through the variable tail current source. As the bandwidth of this amplifier and the buffer stage are equal,  $V[n-1]$  and  $\Delta V[n]$  experience the same delay to reach the input of the sense amplifier. This eliminates any timing issue in the DOM operation. The dynamic offset is proportional to the

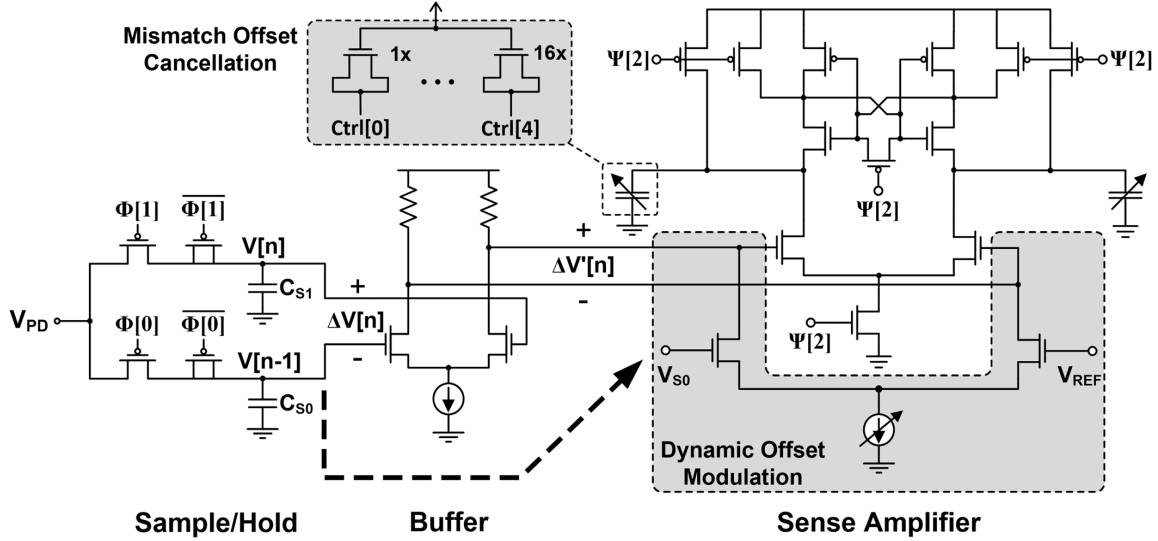


Fig. 7. Detailed schematic of the RC double-sampling front-end.

difference between the sampled voltage ( $V[n-1]$ ) and a reference voltage ( $V_{REF}$ ).  $V_{REF}$  is defined as the average of the maximum ( $V_{DD} - R \times I_1$ ) and minimum ( $V_{DD} - R \times I_0$ ) voltages at  $V_{PD}$ , however, it should be noted that the resulting double-sampled voltage is constant regardless of the  $V_{REF}$  value, as discussed in previous section. Here  $V_{REF}$  only sets the dc value of the double-sampled voltage, that is, with this value for  $V_{REF}$ , the resulting double-sampled voltage changes around zero. As shown in the previous section, the double-sampled voltage is equal to

$$\Delta V_b = \frac{1}{2} R I_1 \left( 1 - e^{-\frac{T_b}{RC_{in}}} \right). \quad (13)$$

For  $T_b \ll RC_{in}$  (13) can be approximated by

$$\Delta V_b \approx \frac{I_1 T_b}{2 C_{in}} = \frac{\rho P_{avg} T_b}{2 C_{in}}. \quad (14)$$

As a result, the receiver sensitivity is a strong function of the bit period ( $T_b$ ), total input capacitance ( $C_{in}$ ), photodiode responsivity ( $\rho$ ), and the total input-referred noise.

$$P_{avg} = \frac{I_1}{\rho} = \frac{2 C_{in} \Delta V_b}{\rho T_b}. \quad (15)$$

The receiver input capacitance is comprised of

$$C_{in} = C_{PD} + C_{pad} + C_{WB} + C_{int} + 2C_S \quad (16)$$

where  $C_{PD}$  is the photodiode capacitance,  $C_{pad}$  denotes the bonding pad capacitance,  $C_{WB}$  is the wirebond capacitance,  $C_{int}$  is the input interconnect capacitance, and  $C_S$  is the total sampling capacitance of each sampler. The required  $\Delta V_b$  is set by minimum signal-to noise ratio (SNR) for target BER and the residual input-referred offset of the sense amplifier after correction  $V_{offset}$ . As a result, the minimum required  $\Delta V_b$  is equal to

$$\Delta V_b = \text{SNR} \times \sigma_n + \frac{V_{offset}}{A} \quad (17)$$

where  $\sigma_n$  is the total input voltage noise variance, which is computed by input referring the receiver circuit noise and the effective clock jitter noise.

The main sources of noise in the RC front-end are the sampler noise, buffer noise, sense-amp noise, and, finally, clock jitter noise, as shown in Fig. 8(a). The single-ended version is shown for simplicity. The sense amplifier is modeled as a sampler with gain and has an input referred voltage noise variance of [9]

$$\overline{\sigma_{SA}^2} = \frac{2kT}{A_{vsa}^2 C_A} \quad (18)$$

where  $C_A$  is the internal sense amplifier node capacitance, which is set to approximately 15 fF in order to obtain sufficient offset correction range. The sense amplifier gain  $A_{vsa}$  is estimated to be equal to near unity for the 0.8-V common-mode input level set by the buffer output, resulting in a sense amplifier voltage noise sigma of 0.75 mV. The buffer noise can be written as

$$\overline{\sigma_A^2} = \frac{2kT\gamma}{C} \quad (19)$$

where  $\gamma$  is the transistor noise coefficient. According to simulation, the input-referred voltage noise variance of the buffer stage is equal to 0.6 mV<sub>rms</sub> while it provides about 6 dB of gain. Sampler voltage noise variance is equal to

$$\overline{\sigma_S^2} = \frac{2kT}{C_S} \quad (20)$$

where the factor of two is due to the two sampling capacitors employed in the sampler block, which generate the differential input voltage to the buffer.

Clock jitter also has an impact on the receiver sensitivity because any deviations from the ideal sampling time results in a reduced double-sampled differential voltage, as shown in Fig. 8(b). This timing inaccuracy is mapped into an effective voltage noise on the input signal with a variance of

$$\overline{\sigma_J^2} = \left( \frac{\sigma_{CLK}}{T_b} \right)^2 \Delta V_b^2. \quad (21)$$

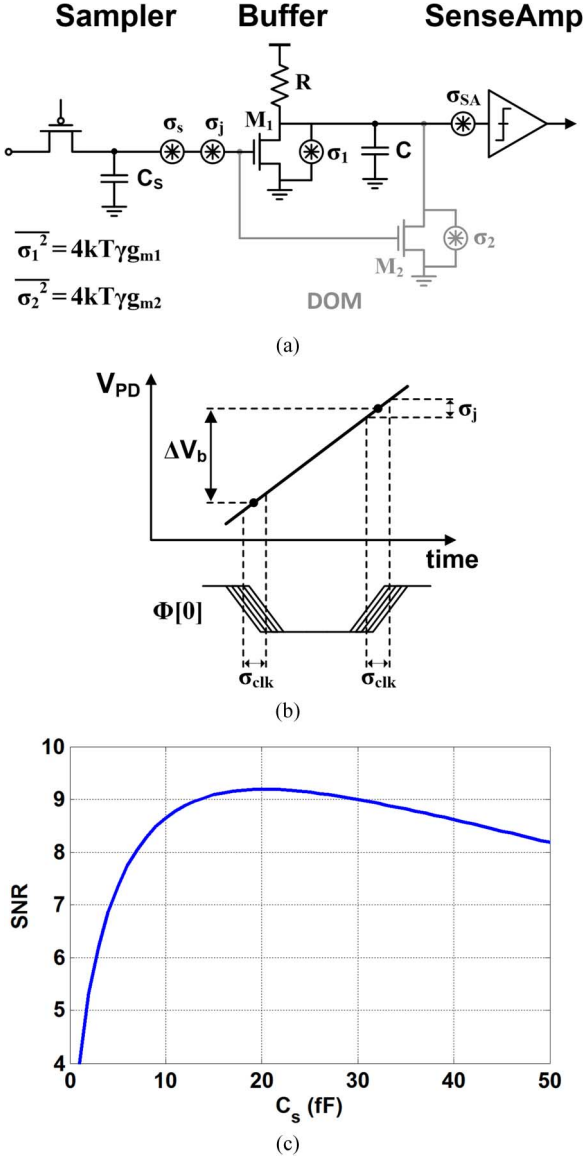


Fig. 8. (a) Schematic showing the noise sources in the front-end. (b) This plot shows how the clock jitter is translated into the double-sampled voltage noise. (c) There is an optimum range, 15–25 fF, for the sampling capacitor to achieve maximum SNR.

Using the measured clock jitter of about  $1 \text{ ps}_{\text{rms}}$ , it is estimated to be about  $0.5 \text{ mV}_{\text{rms}}$ . As shown in Fig. 8(b), DOM also contributes some noise to the system. The total noise due to DOM can be written as

$$\overline{\sigma_{\text{DOM}}^2} = \frac{\beta^2}{2A^2} \left( \overline{\sigma_j^2} + \overline{\sigma_s^2} + 2\overline{\sigma_A^2} \right) \quad (22)$$

where  $A$  is the buffer DC gain. As  $\beta/A \ll 1$ , the noise contribution of the DOM is negligible.

Combining the input-referred circuit noise and effective clock jitter noise, ignoring  $\sigma_{\text{DOM}}$ , results in the total input noise power equal to

$$\sigma_n = \sqrt{\sigma_s^2 + \sigma_A^2 + \frac{\sigma_{\text{SA}}^2}{A^2} + \sigma_{\text{CLK}}^2}. \quad (23)$$

Fig. 8(c) shows how the input SNR changes with the sampling capacitor for an estimated total input capacitance of about 250 fF. The maximum SNR is achieved for  $C_s$  equal to 20 fF. However, a large sampling capacitor requires a large switch size in order to maintain performance at high data rate. This creates a tradeoff between power consumption and data rate as clock buffer power consumption increases with the switch size. As a result in this design we chose  $C_s$  to be about 15 fF to both achieve high SNR and remain in the flat part of the SNR curve to minimize sensitivity to process variation and at the same time reduce the power consumption due to clock buffers. A dummy transistor with half the size of the sampling transistor was also added to the sampler to minimize clock feed-through. In order for the receiver to achieve adequate sensitivity, it is essential to minimize the sense amplifier input-referred offset caused by device and capacitive mismatches. While the input-referred offset can be compensated by increasing the total area of the sense amplifier [16], this reduces the buffer bandwidth by increasing input capacitance and also results in higher power consumption. Thus, in order to minimize the input-referred offset while still using relatively small devices, a capacitive trimming offset correction technique is used [14]. In this technique the capacitance is digitally adjusted to unbalance the amplifier and cancel the offset voltage. The residual offset is limited by the minimum offset cancelling capacitance possible. As shown in Fig. 7, digitally adjustable nMOS capacitors attached to internal nodes and cause the two nodes to discharge at different rates and modify the effective input voltage to the positive-feedback stage. Using this technique, an offset correction range of 60 mV with a residual of 0.9 mV is achieved. The fixed input common-mode voltage provided by the buffers eliminates variability in the offset correction magnitude as the input signal integrates over the input voltage range. The maximum input optical power is set by the requirements of the sampling switches and the transistor oxide breakdown voltage. In order to accurately sample the input voltage in a bit time, on-resistance of the switch should be sufficiently low. Given the 15-fF sampling capacitor, for a 20-Gb/s input, the on-resistance of the transistor should be less than  $1 \text{ K}\Omega$  in order for the resulting time constant to be sufficiently small for the sampled voltage to settle to its final value within a bit interval,  $T_b = 50 \text{ ps}$ . For the employed 65-nm CMOS technology, this translates to a 0.4-V minimum possible voltage at the integrating node  $V_{\text{min}}$ . On the other hand, the maximum possible  $V_{\text{PD}}$  is equal to the oxide breakdown voltage

$$V_{\text{PD max}} - V_{\text{PD min}} = RI_{1 \text{ max}} = R\rho P_{\text{max}}. \quad (24)$$

In this design, the variable resistor ( $R$ ) at the input changes from about 0.8 to  $4 \text{ K}\Omega$ , which allows the receiver to operate for up to 0-dBm input optical power with a photodiode responsivity of about  $1 \text{ A/W}$ . According to simulation, the receiver operates at higher input optical powers as the double-sampled voltage is quite large, however the excessive voltage at  $V_{\text{PD}}$  will stress the transistors connected to this node. The minimum input optical power is determined by the noise performance of the front-end as explained earlier in this section.

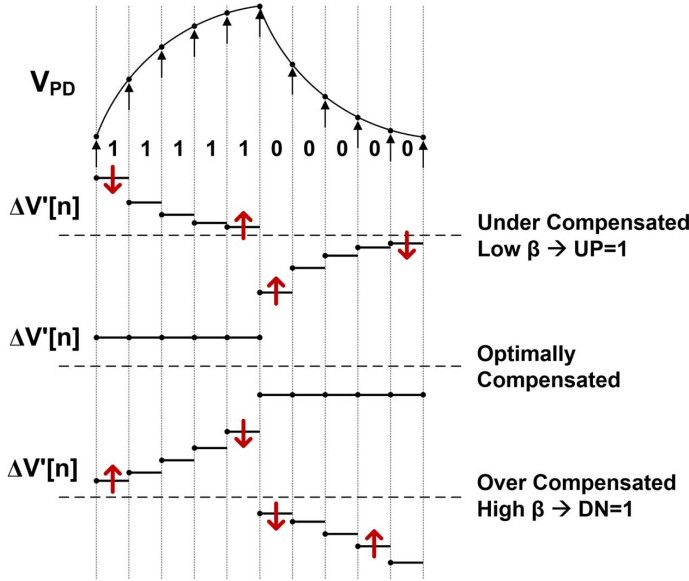


Fig. 9. Basic operation of the DOM gain  $\beta$  adaptation algorithm. The error signal is generated for certain pattern depending on the difference between  $\Delta V[n]$  and  $\Delta V[n-1]$ .

In the fabricated prototype, the DOM coefficient  $\beta$  is adjusted manually. In Section IV, an adaptive algorithm is introduced, which can automatically set  $\beta$  for optimum operation. In addition, the required clock signals are provided from off-chip. In a complete system the clock is generated on-chip using a CDR. In Section IV, we explain how a bang–bang CDR technique can be applied to the proposed receiver.

#### IV. SYSTEM-LEVEL DESIGN CONSIDERATIONS

Here, we will discuss a number of additional design considerations such as adaptation techniques for DOM, scaling behavior of the receiver, and suitable clocking techniques. The feasibility of these techniques is validated through circuit- and system-level simulations.

##### A. Adaptation of DOM

As shown in Section II, the DOM coefficient depends on the front-end time constant ( $RC$ ). As a result, at the beginning of the operation and in order to maintain the operation of the receiver over slow dynamic variations such as temperature or supply drifts, an adaptation technique should be employed. We first consider the  $RC$  front-end without the DOM. As previously discussed and shown in Fig. 9, consecutive ones or zeros generate double-sampled voltages that are not equal. In fact, it is clear that the first bit generates a larger  $|\Delta V[n]|$  than the second bit does. This difference can be employed as an error signal to adjust the DOM coefficient  $\beta$ . In this study, we employ a bang–bang-controlled loop in which the sign of the error signal is used to correct the coefficient with constant steps. The corresponding UP/DN commands can be generated by simply duplicating the comparator part of the  $RC$  front-end. However, the new comparator should compare the two voltage differences. The modified sense amplifier to implement this task is shown in Fig. 10(b).

Fig. 10(a) shows the input voltage waveform of the  $RC$  front-end upon receiving the data. As an example, we choose a “11” data pattern. For this particular pattern, if  $\beta$  is equal to the optimal value, the two double-sampled voltages  $\Delta V[n-1]$  and  $\Delta V[n]$  will be equal. Any error in  $\beta$  would lead to nonequal  $\Delta V[n-1]$  and  $\Delta V[n]$ . The error direction, low or high, determines the sign of the error difference between the two double-sampled voltages for the “11” pattern. Therefore, if each double-sampled voltage is compared with its previous one, the result can be used for  $\beta$  adjustment. The operation is similar to normal data resolution where we compare each sample  $V[n]$  with a one-bit older sample  $V[n-1]$ . Modified comparators, which generate  $P$  signals in Fig. 10(c), are added to the front-end for this purpose. The error information for the adaptation loop is now the difference in the two double-sampled voltages and the 2-b pattern that corresponds to samples  $V[n-1]$  to  $V[n+1]$ . Not all 2-b patterns provide error information for the adaptation loop. The valid patterns are those that give equal  $\Delta V[n-1]$  and  $\Delta V[n]$  when  $\beta$  is adjusted to its optimal value. “11” and “00” are patterns that have such error information. The table in Fig. 10(a) lists valid patterns with the corresponding condition for a meaningful result. Out of four possible 2-b patterns, two give information for adaptation loop. The effective probability of getting phase information from a random input is close to 0.5 when long sequences of ones or zeros do not happen often. Long sequences of ones or zeros result in near zero  $\Delta V[n-1]$  and  $\Delta V[n]$ , which does not provide error information.

A block diagram of a bang–bang-controlled gain adjustment loop is shown in Fig. 10(d). This is a first-order loop and, hence, it is unconditionally stable. From the incoming data, two sets of samplers and comparators resolve the data,  $D$  signals, and raw error information,  $P$  signals. A pattern detector then generates the UP/DN correction commands for the loop. The UP/DN commands are filtered and used to adjust  $\beta$ . For instance, in the case where the  $RC$  time constant was equal to 200 ps and  $T_b = 50$  ps, optimal  $\beta$  is about 0.23 according to (10). As a result, when the loop is closed,  $\beta$  will converge to this quantity, which is also confirmed by closed-loop circuit-level simulations. Fig. 11(a) shows the output of the sampler  $\Delta V[n]$ , when DOM and adaptation circuits are disabled. Applying DOM with the adaptation loop creates a constant double-sampled voltage difference, as shown in Fig. 11(b). The variation in the double-sampled voltage is due to the sampler noise of  $\sigma = 10$  mV incorporated into the simulations. The adaptation loop can be designed to operate only occasionally to correct for slow variations, and the same hardware can be reused for clock recovery as explained in Section IV-C.

##### B. Scaling

Silicon photonics has offered high-performance optical components, such as Germanium photodiodes, waveguides and modulators. This integration allows for very small photodiode parasitic capacitance. Here, we investigate the effect of photodiode capacitance scaling on the performance of the proposed receiver. According to (12), the double-sampling voltage is inversely proportional to the photodiode capacitance. As a result, larger double-sampling voltage can be achieved

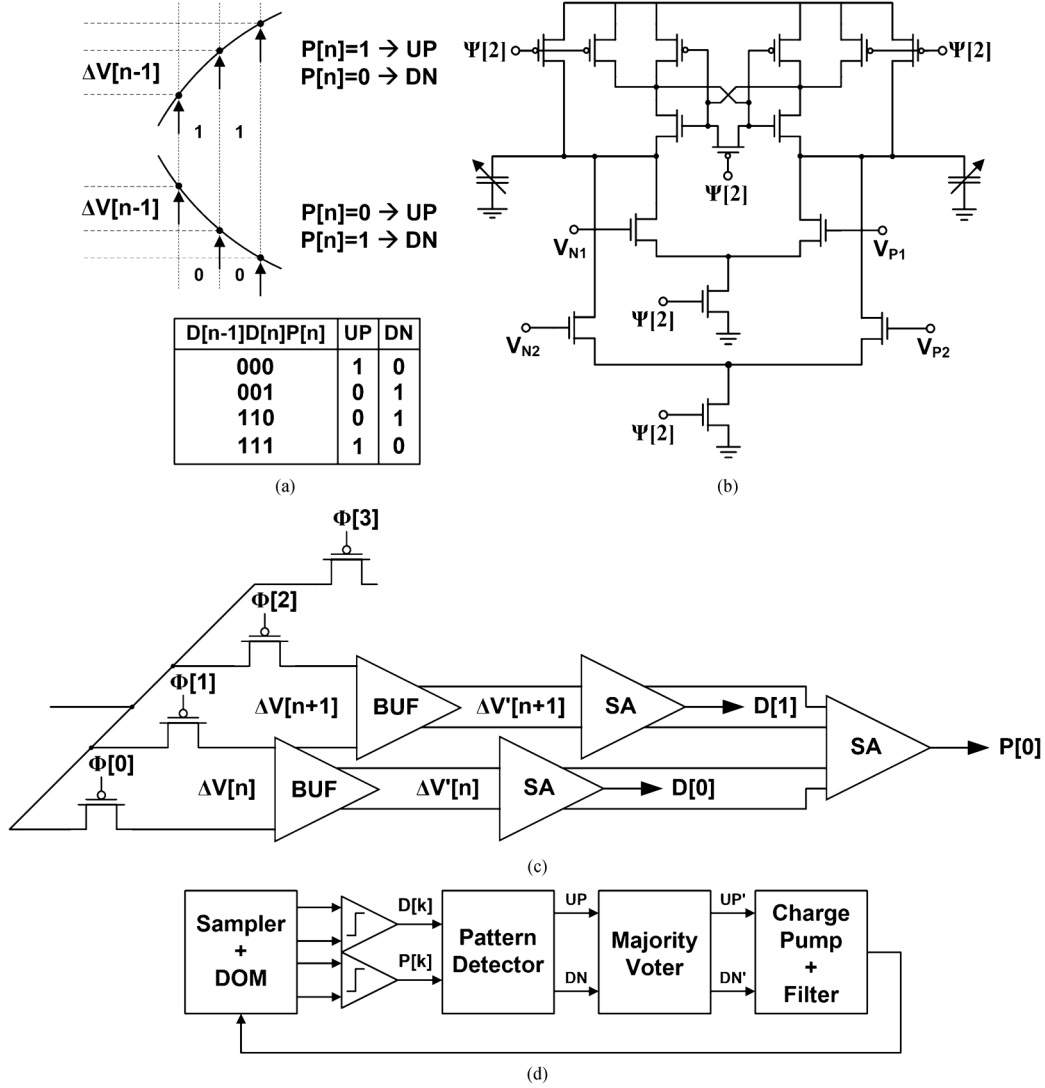


Fig. 10. (a) Input waveform and  $\beta$  error detection. (b) Modified SA as the difference comparator. (c) Samplers and comparators for error detection. (d) Bang-bang  $\beta$  adaptation loop.

using a smaller parasitic capacitance. This allows for scaling the receiver sensitivity  $P_{avg}$  for a fixed data rate. This argument is valid under this assumption that no charge sharing happens between the photodiode capacitance and the receiver sampling capacitors. In order to minimize this charge sharing, a certain ratio between the photodiode capacitance and the sampling capacitor has to be kept. In this design, this ratio is chosen to be about 10. Therefore, while we scale the photodiode capacitance, the sampling capacitor should also scale with the same rate. This in turn increases the  $kT/C$  noise of the sampler and degrades the front-end SNR. However, as the noise is inversely proportional to square root of the capacitor size, the overall SNR and hence the sensitivity of the receiver increases proportional to the square root of the photodiode scaling factor as shown in Fig. 12(a). For instance, in the case of a photodiode capacitance of 50 fF, double-sampling receiver achieves about 34  $\mu A$  of current sensitivity at 20 Gb/s, which improves to 17  $\mu A$  at 10 Gb/s as the integration time is doubled. For an extinction ratio of 10 dB, this translates to about -20-dBm sensitivity. Therefore, the proposed receiver can greatly benefit

in terms of sensitivity from advanced photodiode technologies with small parasitic capacitance and efficient integration techniques such as flip-chip bonding or nanopillars. On the other hand, as the photodiode capacitance scales to 10–20 fF, in the case of monolithically integrated photodiode, the charge sharing between the photodiode capacitance and the sampling capacitance limits the sensitivity of the receiver.

The receiver maximum data rate is also a function of the photodiode capacitance. According to

$$R_b = \frac{1}{T_b} = \frac{\rho P_{avg}}{2C_{in}\Delta V_b} = \frac{\rho P_{avg}}{2C_{in}(SNR\sigma_n + V_{offset})} \quad (25)$$

for a given sensitivity, the data rate ( $R_b$ ) can be increased by scaling the photodiode capacitance.

As mentioned earlier, in order to minimize charge sharing, the sampling capacitor scales with the same rate as the photodiode capacitance. As a result the input referred-noise,  $\sigma_n$ , changes accordingly. For the target RX sensitivity of 100  $\mu A$ , Fig. 12(b) shows how the data rate changes as the photodiode capacitance

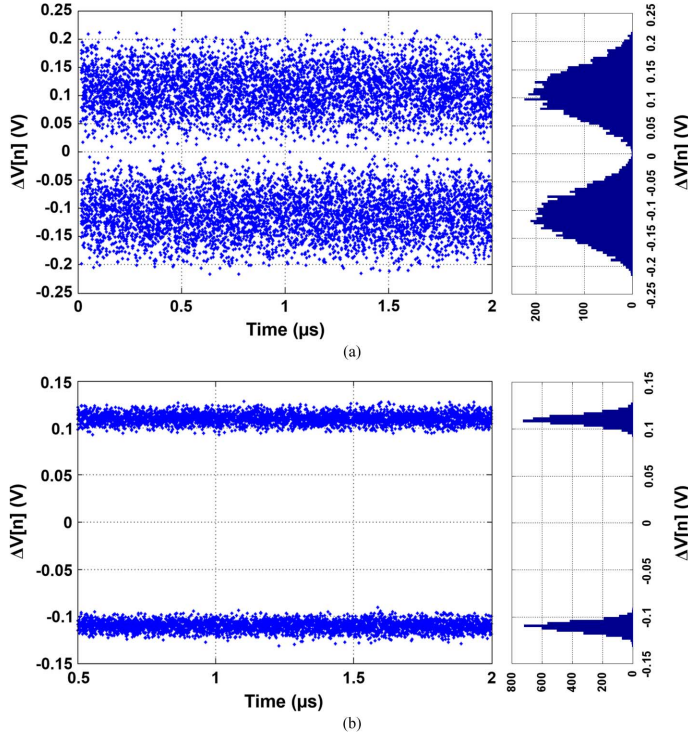


Fig. 11. Simulated performance of the front-end (a) before and (b) after DOM adaptation. Gaussian noise with  $\sigma = 10$  mV is applied at the sampler.

scales. The maximum achievable data rate is ultimately limited by the speed of transistors.

### C. Clocking

An interesting problem in a clocked integrating front-end is to recover the clock from the incoming data. As mentioned in Section III, the clock jitter could be one of the limiting factors in the receiver sensitivity. As a result, an efficient low-jitter clocking technique is crucial. For highly parallel links, a dual-loop CDR [17] can be employed with one loop for the frequency synthesis, which can be shared between all of the channels, and the other for phase correction in each channel (alternatively, in a source-synchronous clocking scheme, the frequency synthesis loop can be eliminated, and a phase correction loop will be sufficient). An alternative technique is to employ a forwarded-clock scheme in a WDM link using one of the channels (wavelengths), which allows for simple phase correction loops to set the optimal sampling time.

The most common phase detection technique employed in electrical signaling is the  $2\times$ -oversampled phase detector known as Alexander phase detector [18]. A similar technique can be applied to the proposed double-sampled front-end. Fig. 13 shows the DOM output voltage upon receiving a one-zero transition. The front-end samples the signal in the middle of each bit-period  $V_m[n]$  and  $V_m[n-1]$ . At any transition, if the clock is in-phase with data, the two samples taken at the middle of these consecutive non-equal bits are expected to be equal. Any phase error would cause these two voltages to be different. This difference can be used as an error signal to adjust the phase of the sampling clocks. In order to implement

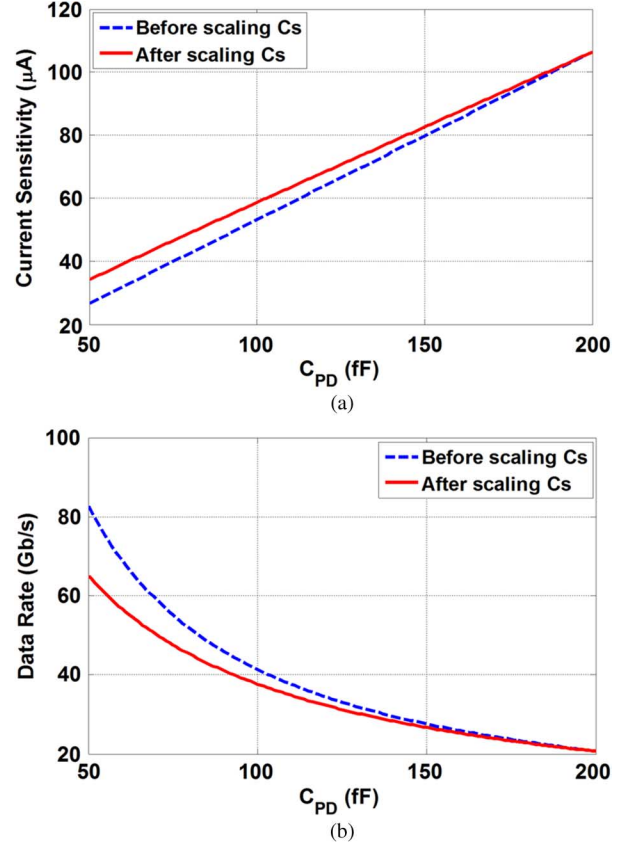


Fig. 12. (a) Receiver current sensitivity versus photodiode capacitance, with and without scaling sampling capacitor. (b) Receiver data rate versus photodiode capacitance for 100  $\mu$ A sensitivity.

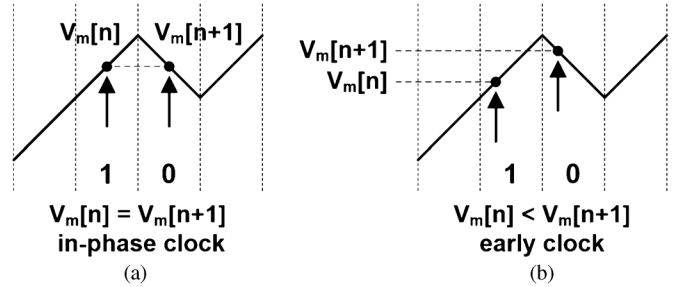


Fig. 13.  $2\times$ -oversampled phase detection for the proposed receiver.

the clock recovery loop, we can duplicate the samplers/comparator part of the front-end. This set of samplers/comparators needs to be clocked with an extra clock phase, shifted by half a bit-period.

Removing the extra phases for oversampled phase recovery can help to reduce the power consumption in the oscillator and clock buffers and relax the difficulties of phase spacing control. The  $RC$  front-end allows us to create an efficient baud-rate phase recovery scheme similar to [9], [19] based only on data samples as shown in Fig. 14. The difference between this method and the one proposed in [19] is that instead of extracting the phase error data from the sampled input, the double-sampled voltage difference at the output of the DOM,  $\Delta V[n-1]$  and  $\Delta V[n]$  in Fig. 14, are employed. This is similar to  $\beta$  adaptation loop except that instead of looking at a 2-b pattern, 4-b patterns are

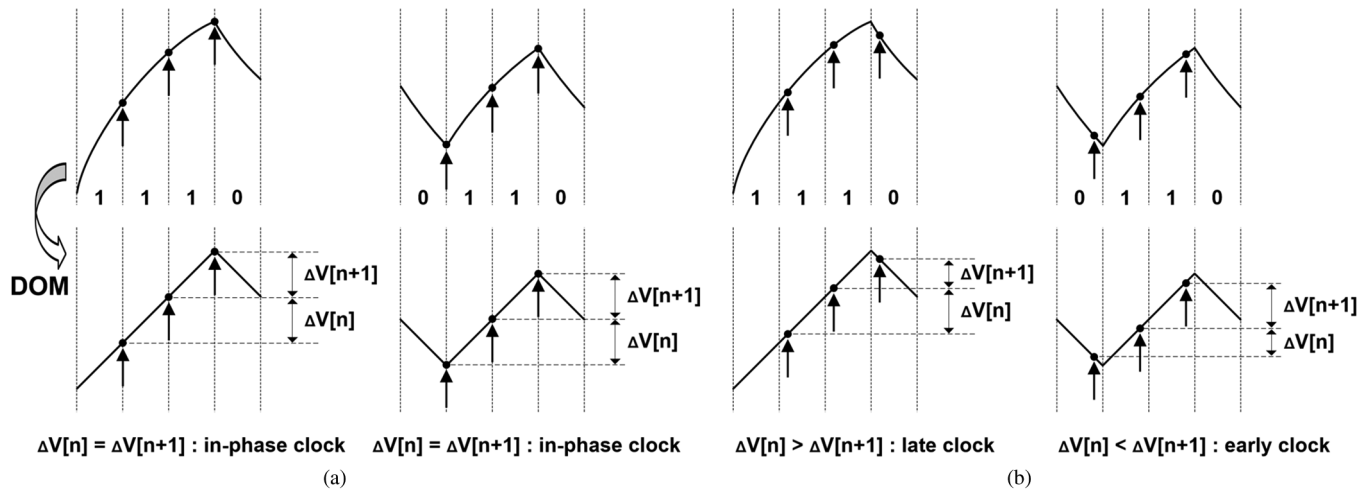


Fig. 14. Input waveform and baud-rate phase detection for (a) in-phase and (b) out-of-phase clock.

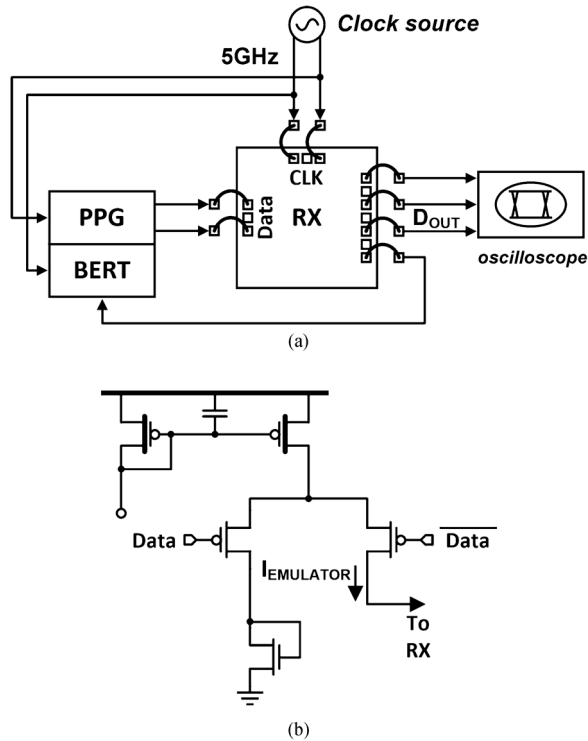


Fig. 15. (a) Electrical measurement setup. (b) Photodiode current emulator.

investigated. As an example, we choose a “0110” data pattern in Fig. 14 to explain the operation of this technique. It is clear from the figure that, for this particular pattern, if the sampling clock is in-phase with the incoming data, then  $\Delta V[n-1]$  and  $\Delta V[n]$  will be equal. Any error in the sampling clock phase would lead to nonequal  $\Delta V[n-1]$  and  $\Delta V[n]$ . The phase error direction, early or late clock, determines the sign of the error difference between the two samples for this pattern. Therefore, if each two consecutive double-sampled voltages are compared, the result information can be used for phase recovery. The valid patterns for phase corrections are those that give equal  $\Delta V[n-1]$  and  $\Delta V[n]$  when the clock is synchronized with the incoming data. “1001” and “0110” are patterns that have complete early/late phase information. Most other patterns have conditional phase information,

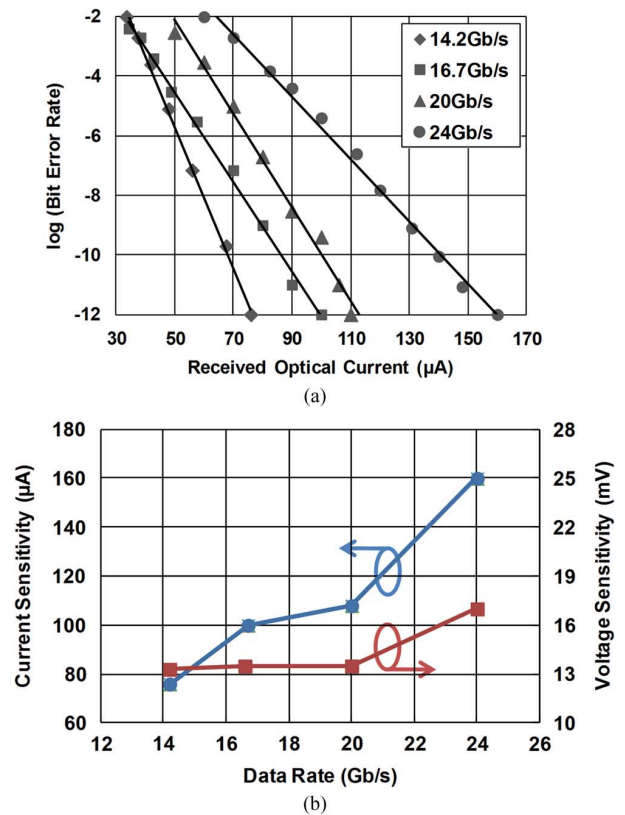


Fig. 16. (a) Receiver sensitivity characteristics for different data rates. (b) Current and voltage sensitivity versus data rate.

e.g. 1110 only gives valid results when the clock leads the input. Due to the less update density in the baud-rate phase detection technique, the overall loop gain is smaller compared to the conventional  $2\times$ -oversampling by almost a factor of 2.67 [19]. As a result,  $2\times$ -oversampling phase correction loop provides higher bandwidth, for identical loop filter and charge-pump, and hence superior jitter tolerance. On the other hand, the baud-rate phase detector has the additional advantage of being less sensitive to clock phase errors, as the same clocks are used for both the data and phase samples, whereas the  $2\times$ -oversampling detector relies on quadrature phase matching.

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

	This work	[4]*	[6]	[8]	[9]*	[10]
Technology	65nm	130nm	65nm	40nm	90nm	130nm SOI
Supply	1.2V	1.8V	1.0	1.0V	1.0V	1.25V
Data Rate	24Gb/s	12.5Gb/s	25Gb/s	10Gb/s	16Gb/s	10Gb/s
Power	0.4pJ/b	3.5pJ/b	3pJ/b	0.4pJ/b	1.4pJ/b	1.5 pJ/b
Area	0.0028mm <sup>2</sup>	0.15mm <sup>2</sup>	0.4mm <sup>2</sup>	-	0.025mm <sup>2</sup>	0.9mm <sup>2</sup>
RX C <sub>in</sub>	>200fF	110fF	-	<60fF	440fF	<20fF
Sensitivity	-4.7dBm**	-8.5dBm***	-7.3dBm	-15dBm	-5.4dBm	NA****

\* Require 8B/10B encoded data to ensure dc balance.

\*\* Coupling loss is not considered @24 Gb/s, about 5 dB loss is expected.

\*\*\* Sensitivity @ 10 Gb/s.

\*\*\*\* 6  $\mu$ A current sensitivity.

Another important aspect of the phase correction loop is its effect on the operation of the  $\beta$  correction loop. As explained earlier, these two loops operate based on the same correction signal  $P$  to minimize the difference between the two consecutive double-sampled voltages,  $\Delta V'[n-1]$  and  $\Delta V'[n]$ . As a result, they can operate concurrently to adjust  $\beta$  and clock phase. This has been validated in simulation for a PRBS7 pattern when the initial phase is about half UI apart from the optimal point. The bandwidth of the  $\beta$  and phase correction loop in this simulation was approximately 2 MHz. This experiment was repeated for the case where the clock phase was leading and lagging with respect to the optimal clock phase as well as undercompensated and overcompensated  $\beta$ .

As mentioned earlier in this section, the only difference between the  $\beta$  adjustment loop and the CDR loop is the length of the pattern that should be monitored. As a result, the same hardware ( $P$  comparators) employed in the  $\beta$  adaptation loop can be reused to perform clock recovery except for the pattern detection logic. This allows for savings in power consumption and area.

## V. MEASUREMENT RESULTS

The prototype was fabricated in a 65-nm CMOS technology with the receiver occupying less than 0.0028 mm<sup>2</sup> as shown in Fig. 15. It is comprised of two receivers, one with a photodiode emulator and one for optical testing with a photodiode. In the first version, an emulator mimics the photodiode current with an on-chip switchable current source and a bank of capacitors ( $C_{PD}$ ) is integrated to emulate the parasitic capacitances due to photodiode and bonding (PAD and wirebond). The four phases of clock are provided from an off-chip signal generator as shown in Fig. 15. An on-chip CML-to-CMOS converter generates the full swing clocks to the receiver. The on chip clock was measured to have about 9-ps peak-to-peak jitter.

The functionality of the receiver was first validated using the on-chip emulator and PRBS7, PRBS9, PRBS15 sequences.  $R$  and  $C_{in}$  were chosen 2.2 K $\Omega$  and 250 fF ( $RC_{in} > 550$  ps). Fig. 16(a) shows how the bit error rate changes with the input current at 14.2, 16.7, 20, and 24 Gb/s. For all these data rates the condition  $T_b \ll RC_{in}$  is valid. The receiver achieves about 75  $\mu$ A of sensitivity at 14.2 Gb/s, which reduces to 160  $\mu$ A at 24 Gb/s. Due to the integrating nature of the receiver, the current sensitivity almost linearly increases with data rate, as shown in

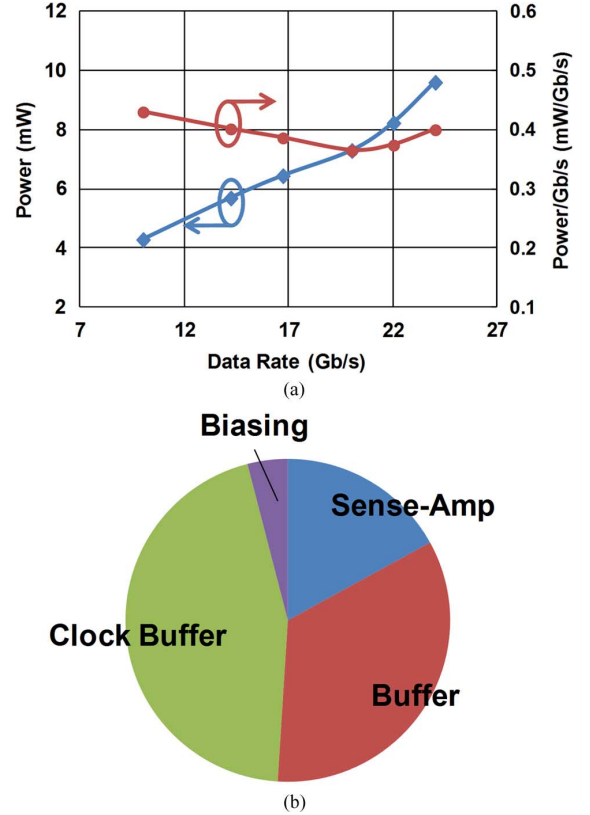


Fig. 17. (a) Power consumption and efficiency at different data rates. (b) Receiver power breakdown.

Fig. 17(b). The voltage sensitivity of the receiver is measured to be about 13 mV up to 20 Gb/s and increases to 17 mV at 24 Gb/s, which is believed to be partly due to degradation of the eye opening at the emulator input. The receiver power consumption (including all clock buffers) at different data rates is shown in Fig. 19. The power increases linearly with the data rate as the receiver employs mostly digital blocks. The receiver offers a peak power efficiency of 0.36 pJ/b at a 20-Gb/s data rate. In order to validate the functionality of the DOM for long sequences of ones or zeros, a 200-MHz square-wave current was applied as the input to the receiver while the front-end sampled the input at 20 Gb/s. In this case, 50 consecutive zeros will be followed by 50 ones. For an input time constant of about 0.55 ns, this number of zeros or ones pushes the input to the flat

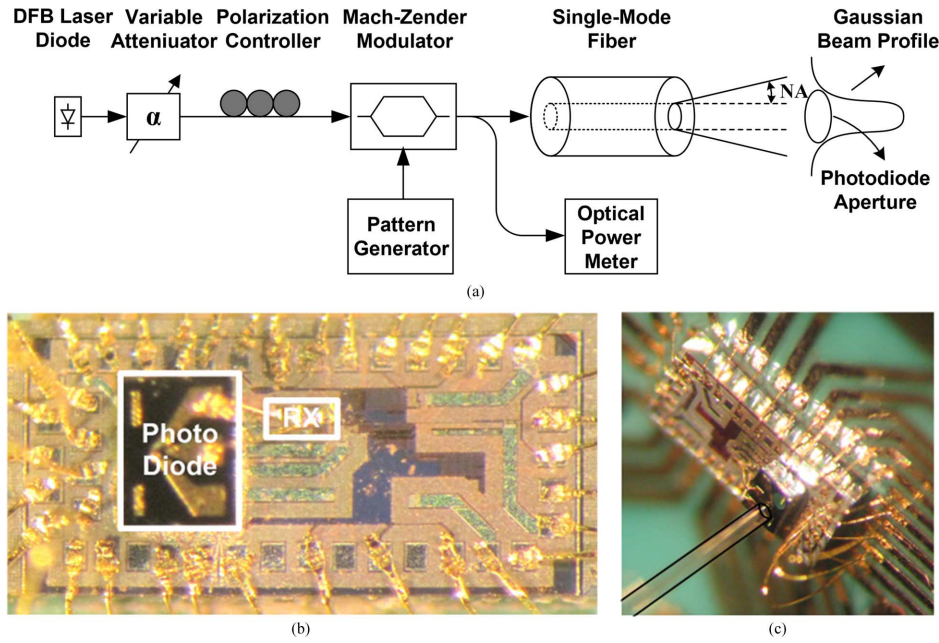


Fig. 18. (a) Optical test setup. (b) Micrograph of the receiver with bonded photodiode. (c) Coupling laser through fiber to the photodiode.

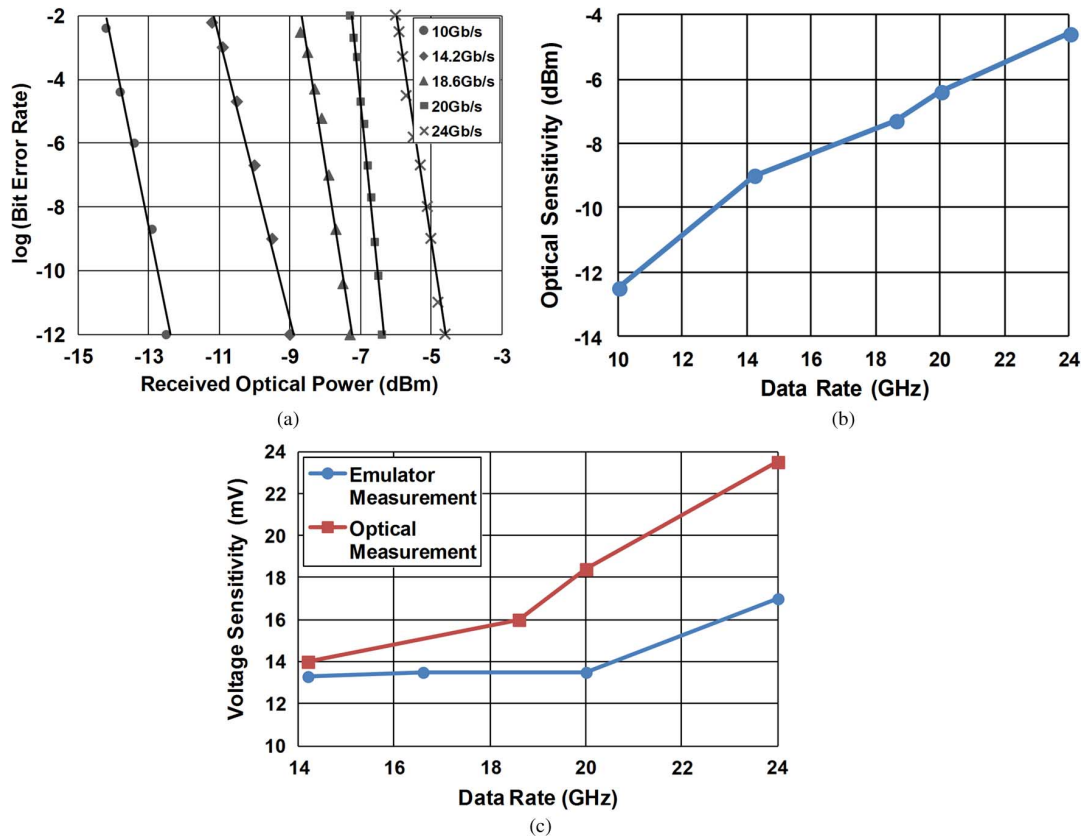


Fig. 19. (a), (b) Optical sensitivity at different data rates. (c) Comparison between voltage sensitivity for electrical and optical measurement.

region were close to zero double-sampling voltage,  $\Delta V'[n]$ , is obtained. Enabling the DOM resulted in error-free detection of the received pattern.

In the second set of measurements, the receiver was wire-bonded to a high speed photodiode and tested at different data rates. The photodiode, bonding pad, wire-bond, and the receiver

front-end are estimated to introduce more than 200-fF capacitance. Fig. 18 shows the optical test setup. The optical beam from a 1550-nm DFB laser diode is modulated by a high-speed Mach-Zender modulator and coupled to the photodiode through a single-mode fiber. The optical fiber is placed close to the photodiode aperture using a micro-positioner. The responsivity of

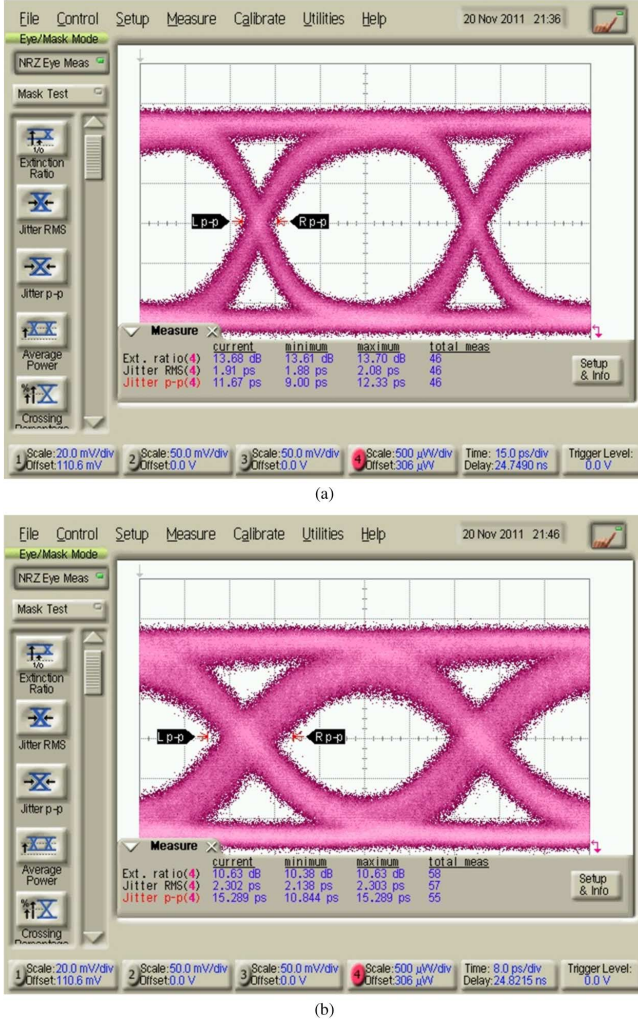


Fig. 20. Optical input eye-diagram to the photodiode at (a) 14 and (b) 24 Gb/s.

the photodiode at this wavelength is about 1 A/W. As the beam has a Gaussian profile, the gap between the fiber tip and the photodetector causes optical intensity loss. This, combined with the optical connectors and misalignment introduce some loss, which can be characterized by comparing the sensitivity in the two experiments. Current and optical power sensitivity are related according to

$$P_S = \frac{\rho I_S}{2} \times \frac{\left(1 + 10^{\frac{-ER}{10}}\right)}{\left(1 - 10^{\frac{-ER}{10}}\right)}. \quad (26)$$

where  $P_S$  is the optical power sensitivity,  $I_S = I_1 - I_0$  is the current sensitivity and ER is the extinction ratio. The measured extinction ratio at 14.2 Gb/s is about 13 dB using the external modulator. As a result, the nominal optical sensitivity according to the current sensitivity of 75  $\mu$ A will be equal to -14 dBm. The difference between the nominal and measured optical sensitivity is about 5 dB, which is believed to be due to the coupling loss. This difference grows as the data rate increases due to the limited bandwidth of the external modulator. Therefore,

the sensitivity can improve by employing advance optical packaging technologies. Fig. 19(a) and (b) shows how the sensitivity of the receiver changes with data rate. Note that the coupling loss is not considered in this plot. The receiver achieves more than -12.5 dBm of sensitivity at 10 Gb/s, which reduces to -7.3 dBm at 18.6 Gb/s and -4.6 dBm at 24 Gb/s. The maximum optical power at which the receiver was tested is 0 dBm. This is the maximum power available from the measurement setup. As mentioned in previous section, the variable resistor at the front-end allows for a wide range of optical input power. For large input optical power the variable input resistor can be reduced to avoid saturation. Fig. 19(c) compares the calculated voltage sensitivity ( $\text{BER} < 10^{-12}$ ) achieved for the electrical and optical input experiments. In both cases, the voltage is calculated by using (14) and the measured current sensitivity. As expected, the sensitivity of the receiver degrades with data rate. In the electrical test the receiver achieves almost constant voltage sensitivity regardless of the data rate. However, for the optical experiment, the calculated voltage sensitivity degrades as data rate increases. The excessive sensitivity degradation in the optical test is due in part to the wire-bonded photodiode and limited bandwidth of the optical modulator, which causes reduced vertical and horizontal eye openings, as shown in Fig. 20. Table I summarizes the performance of the proposed optical receiver and compares it with prior arts.

## VI. CONCLUSION

This paper presents a power-efficient optical receiver in 65-nm CMOS that supports up to 24 Gb/s of data rate. The low-voltage RC front-end receiver uses mostly digital building blocks and avoids the use of linear high-gain analog elements. The proposed receiver employs double-sampling and dynamic offset modulation to resolve arbitrary patterns. An efficient adaptation algorithm for adjustment of DOM gain is proposed and investigated. The application of the baud-rate clock recovery to the receiver is also analyzed. The receiver consumes less than 0.36 pJ/b power at 20 Gb/s, and operates up to 24 Gb/s with -4.7 dBm optical sensitivity ( $\text{BER} < 10^{-12}$ ). Since a large percentage of power consumption is due to the clock buffers and digital blocks [Fig. 17(b)], the overall power consumption can greatly benefit from technology scaling. It is also shown that this design is highly suitable for hybrid integration with low-capacitance photodiodes to achieve high optical sensitivity and high data rate. Experimental results validate the feasibility of the receiver for ultra-low-power, high-data rate, and highly parallel optical links.

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