A 15-Gb/s 0.5-mW/Gbps Two-Tap DFE Receiver With Far-End Crosstalk Cancellation

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***Abstract*—This paper presents a low-power receiver with two-tap decision feedback equalization (DFE) and novel far-end crosstalk (FEXT) cancellation capability, implemented in a 45-nm SOI CMOS process. The receiver employs a half-rate speculative DFE architecture to allow for the use of low-power front-end circuitry and CMOS clock buffers. In the proposed architecture, a switched-capacitor sample-hold at the front-end is employed to perform DFE tap summation. This technique is generalized to implement n taps of equalization. The receiver compensates the effect of crosstalk without making a decision on the received aggressor signal. Due to the low-power nature of the switched-capacitor front-end, the crosstalk cancellation is possible with only 33 μW/Gbps/lane power overhead. The receiver was tested over channels with different levels of loss and coupling. The signaling rate with BER $< 10^{-12}$ was significantly increased with the use of DFE and crosstalk cancellation scheme for highly coupled and lossy PCB traces. The DFE receiver equalizes 15-Gb/s data over a channel with more than 14-dB loss while consuming about 7.5 mW from a 1.2-V supply. At lower data rates it equalizes channels with over 21-dB loss.**

***Index Terms*—Decision feedback equalization (DFE), far-end crosstalk (FEXT), interconnects, receiver, speculative, summation, switched capacitor (SC).**

I. Introduction

MOST advanced electronic systems today require complex architectures that consist of interconnected microprocessors and integrated circuits (IC) such as memory. Examples of such systems are computer servers and high-performance multiprocessor systems. The rapid scaling of CMOS technology continues to increase the processing power of microprocessors and the storage volume of memories. This increases the need for high-bandwidth interconnection between chips, which can be achieved by employing large numbers of input and outputs (IOs) per chip as well as high data rates per IO. Although CMOS scaling has increased the switching speed of transistors, the scaling of interconnect bandwidth has proven to be very difficult. The dielectric and resistive losses of printed circuit board (PCB) traces increase as the operation frequency increases. Such frequency-dependent attenuation causes inter-symbol interference (ISI) and ultimately signal-to-noise-ratio (SNR) degradation. In addition, reflections from discontinuities in the signal path generate more ISI and further reduce the SNR. These problems are exacerbated as the data rate increases.

A common approach in the design of high-speed serial links over bandwidth-limited channels is to employ equalization techniques, including DFE [1]–[9] and continuous time linear equalization [6]–[8] at the receiver and feed-forward equalization (FFE) at the transmitter [10]. These approaches can be used in parallel links with many IOs to increase the aggregate data rate; however, the number of links will be eventually limited by area, noise, and power consumption of the IO. In addition, employing a large number of traces increases the electromagnetic coupling between adjacent traces and results in crosstalk, which degrades SNR at the receiver. A number of techniques have been proposed to remove the effects of crosstalk. The design in [11] employs FFE equalizer and [12] uses crosstalk-induced jitter equalization at the receiver. Other approaches to compensate for crosstalk noise include the use of staggered I/Os [13] or finite-impulse response (FIR) filter at the transmitter [14]. All of these schemes result in significant power consumption and are not suitable for parallel data links.

In this paper, we introduce a low-power DFE receiver with crosstalk cancellation capability. The organization of the paper is as follows. In Section II, we introduce the receiver architecture. In Section III, the DFE design including the switched-capacitor (SC) summation technique and how it can be extended to a large number of equalization taps for high-loss channels is presented. Section IV focuses on the crosstalk cancellation scheme. In this section, we explain how crosstalk can affect the performance of the link and present a novel technique to cancel this effect with low power overhead. Experimental results from the evaluation of the receiver implemented in a 45-nm SOI CMOS process are presented in Section V, where the performance of the receiver operating over a variety of channels is discussed.

II. Receiver Architecture

A diagram of a typical parallel communication link is shown in Fig. 1. Many ICs are connected via PCB traces. The loss in these traces, as well as the electromagnetic crosstalk due to adjacent traces, significantly degrades the signal integrity in such systems. A common approach to removing the ISI induced by the bandwidth-limited channel is to employ DFE at the receiver. This technique helps to compensate for post-cursor ISI arising from the spread of a single pulse over time. Fig. 2 shows the top-level architecture of the proposed two-tap DFE receiver. In the DFE, weighted versions of previous bits are added to or subtracted from the main sample by a summer at the front-end. As shown in Fig. 2, in a two-tap DFE, the ISI from previous bits is compensated by adjusting taps H_1 and H_2. To avoid timing

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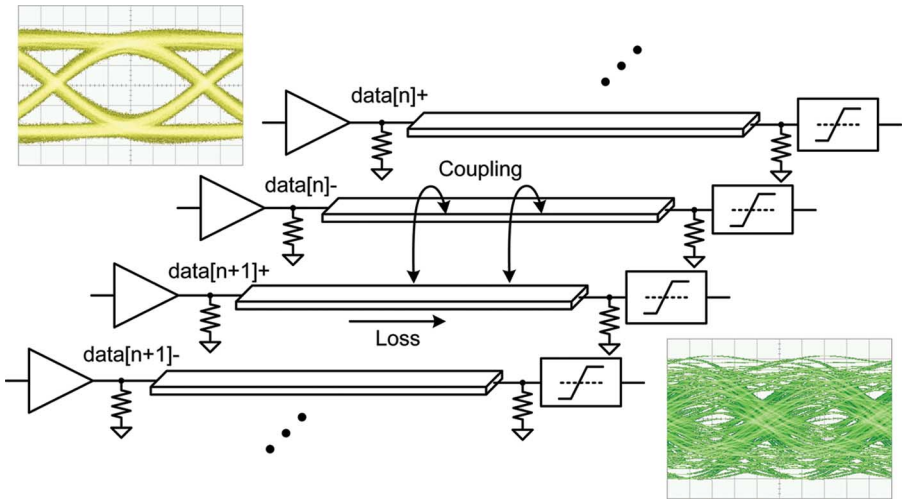


Fig. 1. Signal integrity degradation due to channel loss and crosstalk talk noise of the neighboring signal.

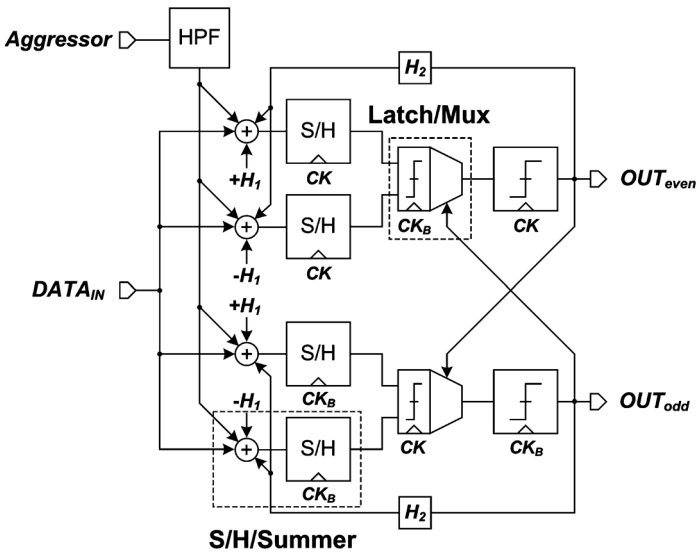


Fig. 2. Top level architecture of the half-rate loop-unrolled receiver with crosstalk cancellation.

issues in the first tap equalization path, a speculative DFE architecture is employed, in which the outcomes for both possible values (one and zero) of the previous bit are fully resolved to digital levels. A multiplexer then chooses the correct value based on the resolved previous bit. Therefore, two clocked latches are required to restore the digital levels. The design employed in this paper uses a combined analog multiplexer and latch to select one of the two analog voltages directly at the output of the summer and resolve the digital bit [1]. The power consumption associated with latches is reduced since a single latch is embedded into the multiplexer, as shown in Fig. 2. In this design, a half-rate clocking technique is adopted to further reduce power consumption. This approach helps to relax the DFE timing constraint and the design requirements of the clocking and the slicers. It also helps to save power in the following digital de-multiplexing stages. Crosstalk cancellation in the proposed design is performed via a novel, low-power technique in which the aggressor signal is used to reproduce the coupling noise, as shown in Fig. 2. Further details of this technique will be provided in Section IV.

III. Decision Feedback Equalization Implementation

As discussed in the previous section, in a DFE, it is necessary to add weighted information from previous bits to the received signal to make a decision on the current bit. At high data rates, the design of a linear and precise summer that meets the DFE timing requirement is challenging. Conventionally, taps of the equalizer are implemented using current-mode summers, thus the power consumption of the DFE increases proportionally with the number of taps. The extra capacitance due to equalization taps also introduces additional loading at the summer output and limits its bandwidth.

Here, we first introduce a four-tap realization of the proposed SC summer, in which two taps are employed for equalization and two taps for crosstalk cancellation. Then, we show how this technique can be generalized to implement n taps of equalization. In the proposed architecture, an SC front-end, which is denoted as S/H/Summer, is employed to sample the input signal and combine it with the feedback coefficients as shown in Fig. 2. Fig. 3(a) shows the implementation of the S/H/summer. The single-ended version is shown for simplicity. The S/H/summer operates in two phases, shown in Fig. 3(b) and 9c). In the first, sample/sum phase, the input is sampled into capacitor $C_{\rm S1}$ and the first tap coefficient, $\mathrm{H}_1 = \alpha_1 V_{\rm REF}$, is added to (or subtracted from) this sample. During this phase, as will be discussed later, the crosstalk canceling signal is stored into capacitor $C_{\rm S2}$. As a result, at the end of this phase, the voltage across $C_{\rm S1}$ and $C_{\rm S2}$ will be respectively equal to

$$V_{\rm CS1} = \alpha_1 V_{\rm REF} - V_{\rm IN} \tag{1}$$

$$V_{\rm CS2} = V_{\rm CM} - V_{\rm X-TALK} \tag{2}$$

where $V_{\rm X-TALK}$ is the mimicked crosstalk noise, explained in Section IV, $V_{\rm CM}$ is the common-mode voltage, and $V_{\rm IN}$ is the input signal. In the second, sum/hold phase, the result of the first phase is added to the second tap coefficient $\mathrm{H}_2 = \alpha_2 V_{\rm REF}$ and applied to the next stage comparator. This is done by putting the

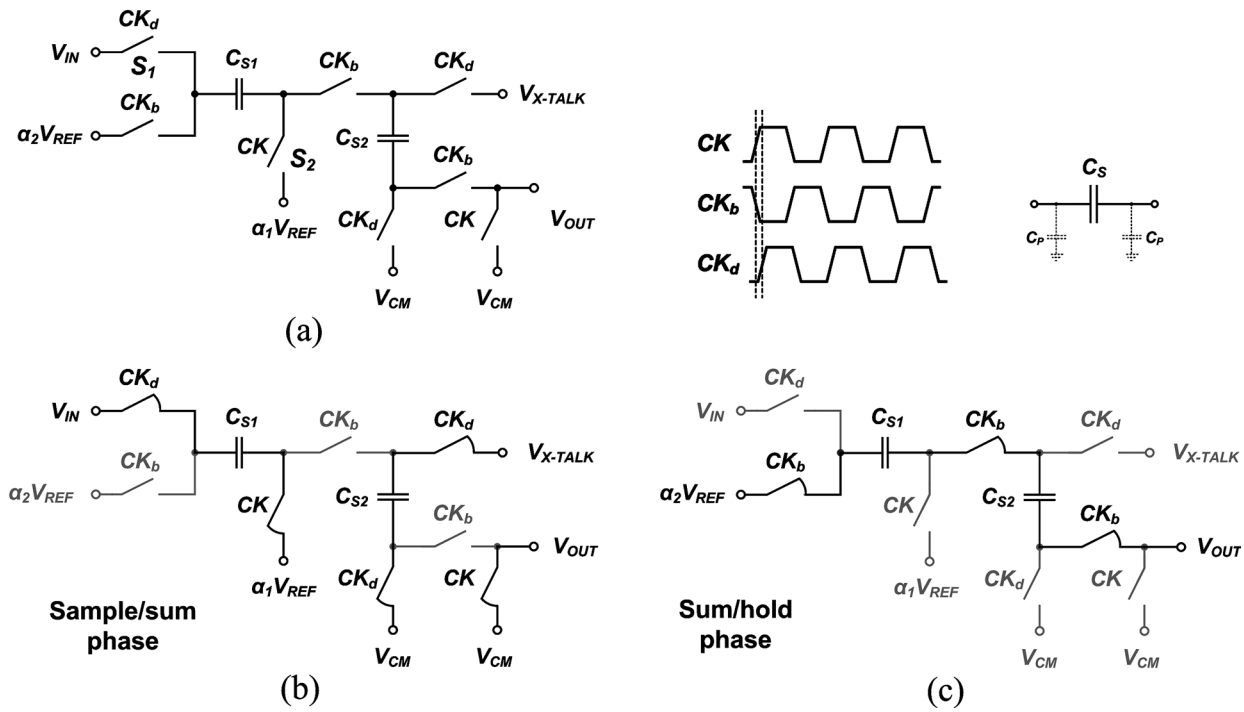


Fig. 3. (a) Circuit-level implementation of the front-end S/H/summer operating in two phases: (b) sample/sum phase (c) sum/hold phase (single-ended version is illustrated for simplicity).

two sampling capacitors in series which results in the output to be equal to

$$V_{\rm OUT} = \alpha_2 V_{\rm REF} + V_{\rm CS1} + V_{\rm CS1} = \alpha_1 V_{\rm REF} + \alpha_2 V_{\rm REF} + V_{\rm CM} - V_{\rm IN} - V_{\rm X-TALK}. \quad (3)$$

In order to minimize input-dependent charge injection, the switch that connects the sampling capacitor to the input, $\rm S_1$, is turned off slightly after $\rm S_2$. This is possible through employing the delayed version of the clock, $\rm CK_d$.

A key aspect of the design of the SC DFE is the sizing of the sampling capacitors. Optimizing this sizing demands an understanding of how loss, SNR, and power change as a function of the sampling capacitor size, requiring an analysis of how it affects parasitic capacitance, receiver noise, and clocking power. When this technique is implemented with capacitors and switches, the parasitic capacitances, shown in Fig. 3 as C_p, cause signal gain degradation due to charge sharing. Therefore, the resulting gain from the input to the S/H/Summer output is equal to

$$A_{\rm sampler} = \frac{C_{s1}C_{\rm s2}}{(C_{\rm s1} + C_{\rm s2} + 2C_p)(C_{\rm s2} + C_p + C_L) - C_{\rm S2}^2} \quad (4)$$

where $A_{\rm sampler}$ is the signal gain, C_p is the parasitic capacitance, and C_L is the load capacitance from the next stage. C_p is due to the switch junction capacitance, sampling capacitors top and bottom plate parasitic, and the wiring capacitance. As a result, it almost linearly changes with the sampling capacitor size. Fig. 4(a) shows how the signal gain changes with the sampling capacitors sizes for the proposed four-tap S/H/Summer. The loading from the next stage (slicer/MUX) is estimated to be about 2 fF. The sensitivity of the receiver is mainly determined by the performance of the front-end S/H/summer. In order to achieve reasonable SNR, the signal loss and the noise must be kept as low as possible. Contributing to the input-referred circuit noise are the slicers and samplers in the receiver. The slicer is modeled as a sampler with gain and has an input referred voltage noise variance of [15]

$$\sigma_{\rm slicer}^2 = \frac{2kT}{A_{\rm slicer} \times C_A} \quad (5)$$

where C_A is the total capacitance at the internal slicer node ($V_{\rm int}$ in Fig. 7), which is approximately 8 fF. $A_{\rm slicer}$ is the gain from the input of the slicer to the internal node, $V_{\rm int}$, which is estimated to be equal to two. This results in a slicer voltage noise sigma of 0.5 $\rm mV_{rms}$. Sampler voltage noise variance is equal to

$$\sigma_s^2 = \frac{2kT}{C_{s1}} + \frac{2kT}{C_{s2}}. \quad (6)$$

Clock jitter also impacts the receiver sensitivity because any deviation from the ideal sampling time results in a reduced sampled voltage. This timing inaccuracy is mapped into an effective voltage noise on the sampled input signal with a variance of

$$\sigma_{clk}^2 = \sigma_j^2 \times R_b^2 \quad (7)$$

where $\sigma_{\rm j}$ is the clock jitter and R_b is the rate of the input voltage change around the sampling point. The timing noise is estimated to be equal to 0.75 $\rm mV_{rms}$. The total noise is equal to

$$\sigma_n = \sqrt{\sigma_{slicer}^2 + \sigma_s^2 + \sigma_{\rm clk}^2} \quad (8)$$

which results in SNR equal to

$$\rm SNR = \frac{V_b \times A_{sampler}}{\sqrt{\sigma_{slicer}^2 + \sigma_s^2 + \sigma_{clk}^2}} \quad (9)$$

where V_b is the eye opening amplitude after equalization taps are applied. Simulation shows that if a 400-mVpp differential input at 15 Gb/s is transmitted over a 5-in FR-4, 40 mV of eye opening amplitude is generated using two taps of equalization. Replacing $V_b = 40$ mV in (9) results in the S/H/summer SNR plot shown in Fig. 4(b). The SNR increases with the sampling capacitor sizes. However, in order to maintain bandwidth, the corresponding switch size also has to be increased, which affects the sampler performance by adding more parasitic capacitance and hence increasing the signal loss. Furthermore, to drive a large switch, a large clock buffer is required that increases the overall power consumption. This power is proportional to the capacitance driven by the buffers. If we ignore the capacitance introduced by the buffer itself, the total clock buffer power consumption can be written as

$$P_{\rm clk} = KC_{\rm s-tot}V_{\rm dd}^2 f + KC_{\rm slicer}V_{\rm dd}^2 f \tag{10}$$

where k is the activity factor equal to 0.5 for clock buffers, $C_{\rm s-tot}$ is the total capacitance introduced by the S/H/Summer switches, $C_{\rm slicer}$ is the capacitance in the slicer that is driven by clock buffers, and f is the operating frequency. Fig. 4(c) shows the SNR normalized to the power consumption of the clock buffers. We employed this metric, along with the SNR, to choose the sampling capacitor sizes. In order to achieve BER $< 10^{-12}$(SNR > 7.1) and low clocking power consumption in this design, the sampling capacitors $(C_{\rm S1}, C_{\rm S2})$ are optimized to be about 20 fF; however, in order to meet the settling time requirements within a bit interval, according to simulations, $C_{\rm S1}$ and $C_{\rm S2}$ are chosen to be equal to 19 and 14 fF, respectively. As the $\rm SNR/P_{clk}$ is quite flat around the maximum point, the SNR and power penalty is small.

Two 4-b current-steering digital-to-analog converters (DACs) generate the differential equalization coefficients $(\alpha_1 V_{\rm REF}, \alpha_2 V_{\rm REF})$ as shown in Fig. 5. In this work, equalization tap coefficients are adjusted manually, however, on-chip adaptation algorithms such as SS-LMS and BER-based adaptation [16] can be utilized to optimize the tap values. The two DACs are designed to deliver sufficient current drive without considerable voltage drop while consuming less than 900 μA. A 1-pF bypass capacitor at the DAC output filters noise and kickback charge from the switches. During each bit interval, the DAC should charge/discharge one sampling capacitor, $C_S \approx 20$ fF, from the S/H/Summer, which causes a very small charge sharing with the bypass capacitor. In a differential implementation, the voltage change due to charge sharing appears as a common-mode noise to the first order and, hence, does not affect the DFE performance significantly.

The SC summation technique can be further extended to realize a large number of taps. Fig. 6(a) and (b) shows the operation of a $2n$-tap S/H/Summer, where $\alpha_{\rm k} V_{\rm REF}$ represents the weighted version of the kth previous bit. In the first phase, the input and $2n-1$ taps of the DFE $(\alpha_1 V_{\rm REF}, \ldots, \alpha_{2n-1} V_{\rm REF})$ are sampled and stored over n sampling capacitors $(\rm C_{S1}, \ldots, C_{Sn})$. The capacitors are connected in series in the second phase, as shown in Fig. 6(b) where one side is connected to the $2n^{\rm th}$ tap coefficient, $\alpha_{2n} V_{\rm REF}$, and

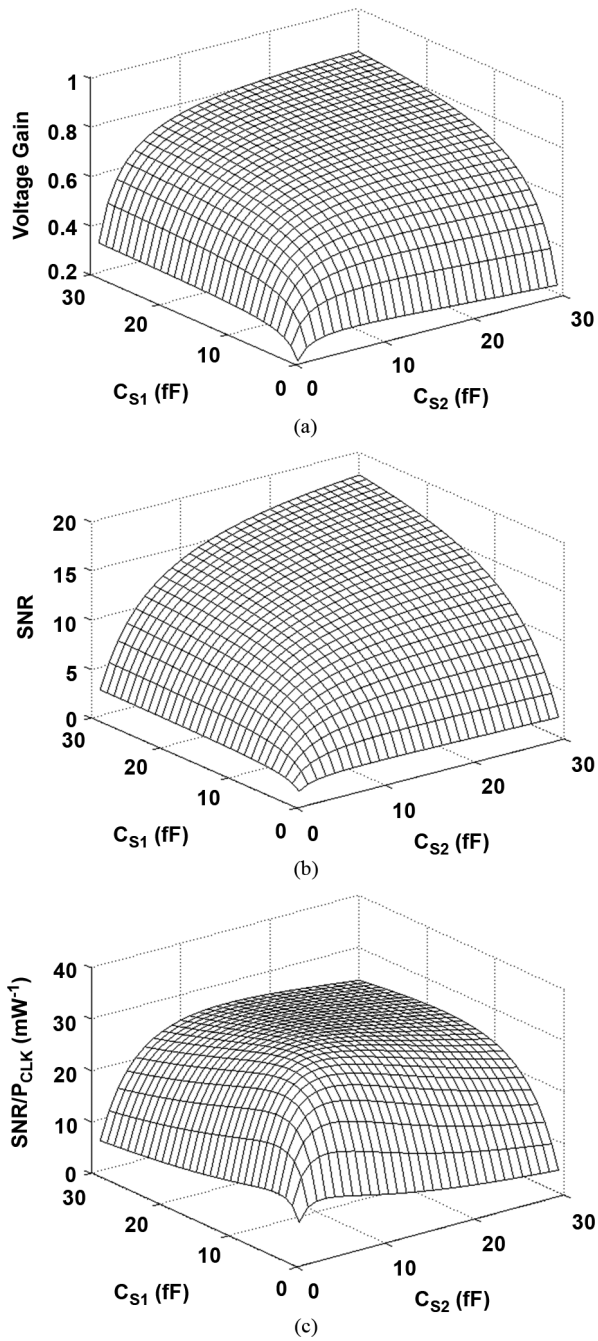


Fig. 4. S/H/summer performance in the case of $n = 2$. (a) S/H/summer voltage loss, $A_{\rm sampler}$. (b) SNR at the output of the S/H/summer. (c) SNR normalized to clocking power consumption. To achieve high SNR (hence high BER) and power efficiency while maintaining the DFE speed, $C_{\rm S1}$ and $C_{\rm S2}$ are chosen to be equal to 19 and 14 fF, respectively.

the other side is the output of the S/H/Summer. The resulting output at the end of the second phase is equal to

$$\begin{aligned} V_{\rm OUT} =& V_{\rm IN} + (\alpha_2 V_{\rm REF} + \cdots + \alpha_{2n} V_{\rm REF}) \\ & - (\alpha_1 V_{\rm REF} + \cdots + \alpha_{2n-1} V_{\rm REF}) \end{aligned} \tag{11}$$

which is the sum of the sampled input and all feedback coefficients. Coefficients can be negated simply by swapping the differential signals in a differential implementation. As mentioned

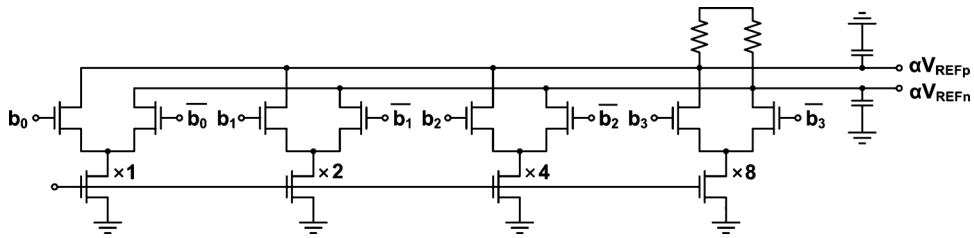
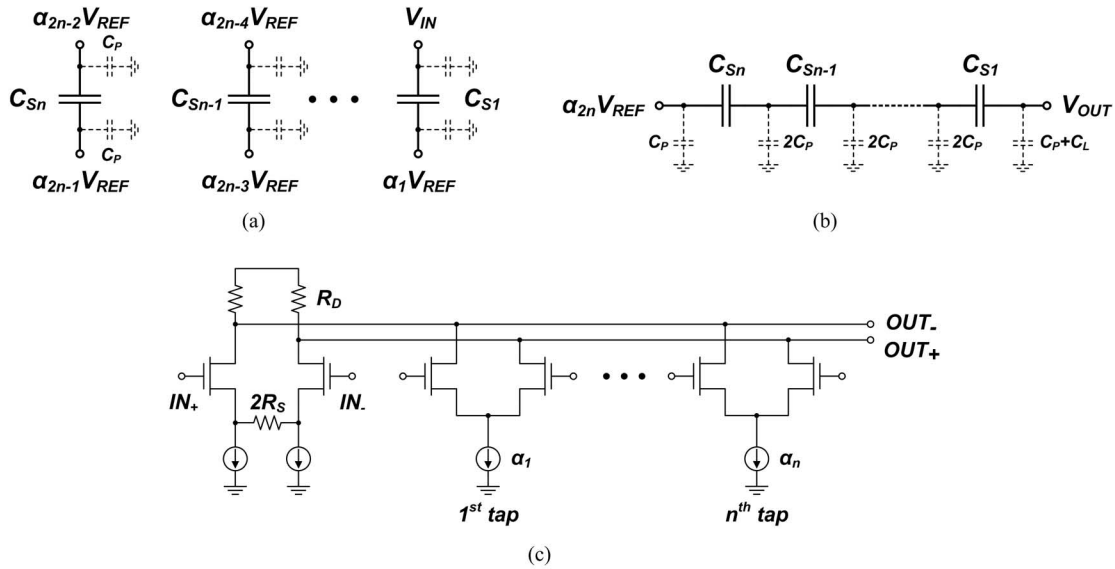


Fig. 5. 4-b current-steering DAC that generates DFE tap coefficients.



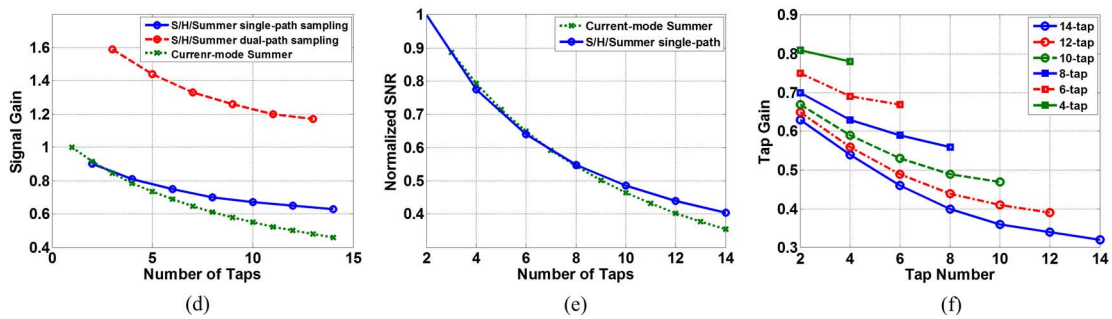


Fig. 6. SC summer for $2n$-tap, operating in two phases. (a) Sample/sum phase. (b) Sum/hold phase. (c) Current-mode summer with n equalization taps. (d) Signal gain comparison between SC and current-mode summer. (e) Normalized SNR for the SC and current-mode summer. (f) Tap coefficient gain for different number of taps.

earlier, due to charge sharing between the sampling capacitors and the parasitics, the voltage gain in practice will be less than unity. In order to minimize the effect of parasitics and charge sharing on gain, the capacitor that samples the input signal is chosen to be the last capacitor in the chain, C_{S1}. Fig. 6(d) shows how the voltage gain decreases with increasing the number of taps. In order to compensate for the voltage gain degradation for a larger number of taps, the input can be sampled using two sampling capacitors, which results in a factor of 2 increase in voltage gain, as shown by the dashed line in Fig. 6(d). We denote this technique as dual-path sampling. The factor of 2 increase in gain comes as a result of sacrificing one of the DFE taps to sample the input. It also increases the input loading, but, since the input is 50-Ω terminated, the additional loading due to the extra sampling capacitors has a negligible effect on the overall channel insertion loss. On the other hand, the sampling capacitors can be sized smaller to compensate for the loading effect. Scaling the sampling capacitors results in parasitic reduction and hence charge sharing effect remains the same. As noise is proportional to the square root of the capacitor size, the same input loading can be achieved by reducing the sampling capacitors by a factor of 2 and still achieving $\sqrt{2}$ improvement in SNR. This also helps decreasing the clocking power consumption as smaller switches are required for a given data rate. For comparison purpose, Fig. 6(c) shows the current-mode summer conventionally employed for tap summation in DFE designs. The summer voltage gain is equal to

$$A = \frac{R_D}{\frac{1}{g_m} + R_S}. \tag{12}$$

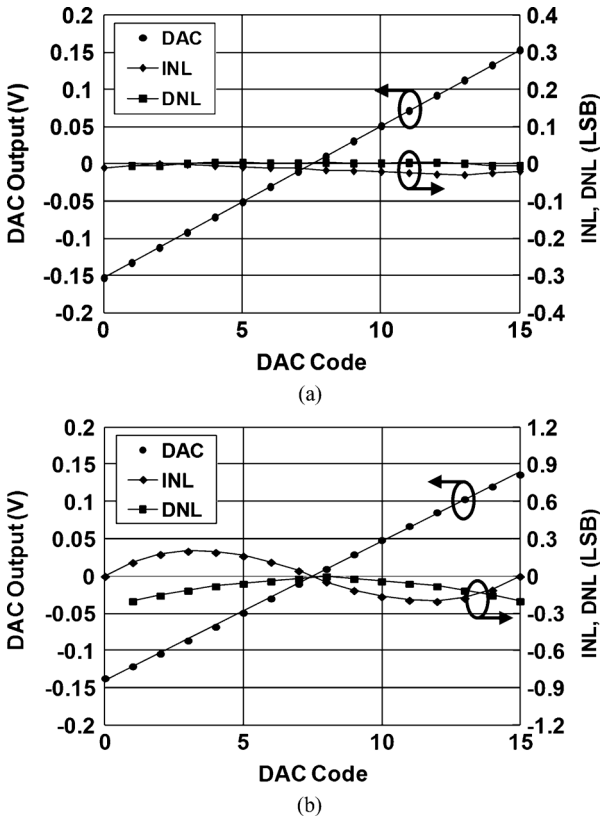


Fig. 7. Linearity of the post-cursor taps for an eight-tap (a) SC and (b) current mode summer.

where $\mathrm{g_m}$ is the input transistor transconductance. To maintain the bandwidth while increasing the number of taps, load resistance should be reduced. This causes the voltage gain to decrease for a constant $\mathrm{current}/g_m$ in the main tap. The dotted line in Fig. 6(d) shows how the voltage gain changes by increasing the number of taps while keeping the main tap current constant assuming each tap adds ten percent extra capacitance to the summing node [8]. To maintain the voltage gain and the bandwidth regardless of the number of taps, larger g_m and hence more power consumption is required in this technique. The reduction in voltage gain due to increasing the number of taps affects the receiver sensitivity by degrading the SNR. Fig. 6(e) shows the normalized change in the front-end SNR with the number of DFE taps for the SC and current-mode summers. For the current-mode summer it is assumed that any additional tap contributes ten percent of the original noise [8]. Another important aspect of the post-cursor tap summer is its linearity. As the gain of the summer for each tap is determined by the ratio of capacitors, the only source of nonlinearity is the parasitic capacitors introduced by transistor switches. For the tap voltage range that the SC summer operates, simulation shows that the parasistic capacitance (due to junction capacitance) changes about 10%. However, as mentioned earlier, the parasitic capacitance is comprised of sampling capacitor parasistics, interconnects, and switches. As a result, the overall parasitic capacitor change is less than 5%. Fig. 7(a) shows the linearity simulation results for an eight-tap SC summer, including the tap coefficient DAC. In the current-mode summer the main source of nonlinearity is

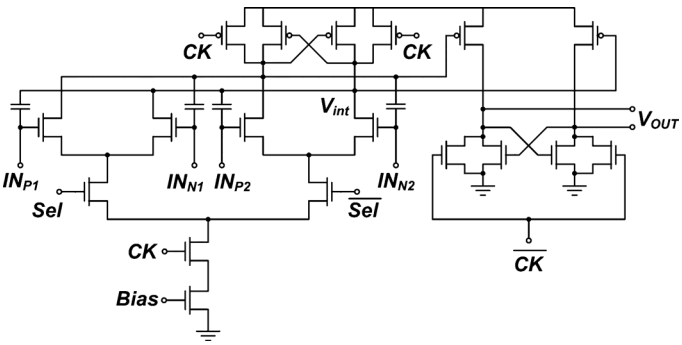


Fig. 8. Combined Analog MUX and latch with cross-coupled capacitors to reduce kickback.

due to the tail current source that generates α_n. As the tap differential pair transistors are sized small to add minimum parasitic to the output node, at high currents, the voltage across the tail current source reduces drastically. This causes reduction in the tail current due to channel length modulation. Fig. 7(b) shows the linearity simulation results for an eight-tap current-mode summer where each tap transistor size is about 10% of the main tap to minimize loading [8] (both in Fig. 7(a) and (b), transistor mismatch is not accounted for).

The tap coefficients gain in SC implementation is also a function of both number of taps and the tap number. Fig. 6(f) shows how the tap gains change with the number of taps and also the tap number. The tap sampled by the first capacitor in the chain, C_{Sn}, experiences larger loss compared with the taps sampled by the last capacitor in the chain, C_{S1}. As a result, the DAC that generates α_{2n-1} should provide a larger voltage compared to that of α_1. On the other hand, post-cursors generated in a realistic channel decay with the tap number, that is, α_{2n-1} is inherently smaller than α_1. This can compensate the lower gain of the tap coefficients sampled by the first capacitors in the chain.

Fig. 8 shows the slicer combined with the analog MUX, which was explained in Section II. Since the MUX is clocked with full-swing clock signals, the clock switch transistors are operating in the linear region, and the stacking of the transistors is easier given the limited voltage supply. In addition, as the tail transistor and the MUX transistors are not in the DFE critical loop, they can be sized to be relatively large to allow for proper operation of this stage at low supply voltages. In order to cancel the kickback from the latch output to the sensitive sampling nodes, small metal capacitors cross-couple the output and the input. These capacitors also reduce the loss of the S/H/summer due to the charge sharing between the sampling capacitors and the slicer/MUX input parasitic capacitor as they cancel the Miller capacitance associated to the gate–drain capacitance of the input differential pair.

IV. Crosstalk Cancellation

FEXT in transmission lines is a signal that is electromagnetically coupled from one line (aggressor line) to another line (victim line) and is received at the end of the victim line. It appears as an interfering signal at the victim channel receiver and degrades the horizontal and vertical eye-opening of the original

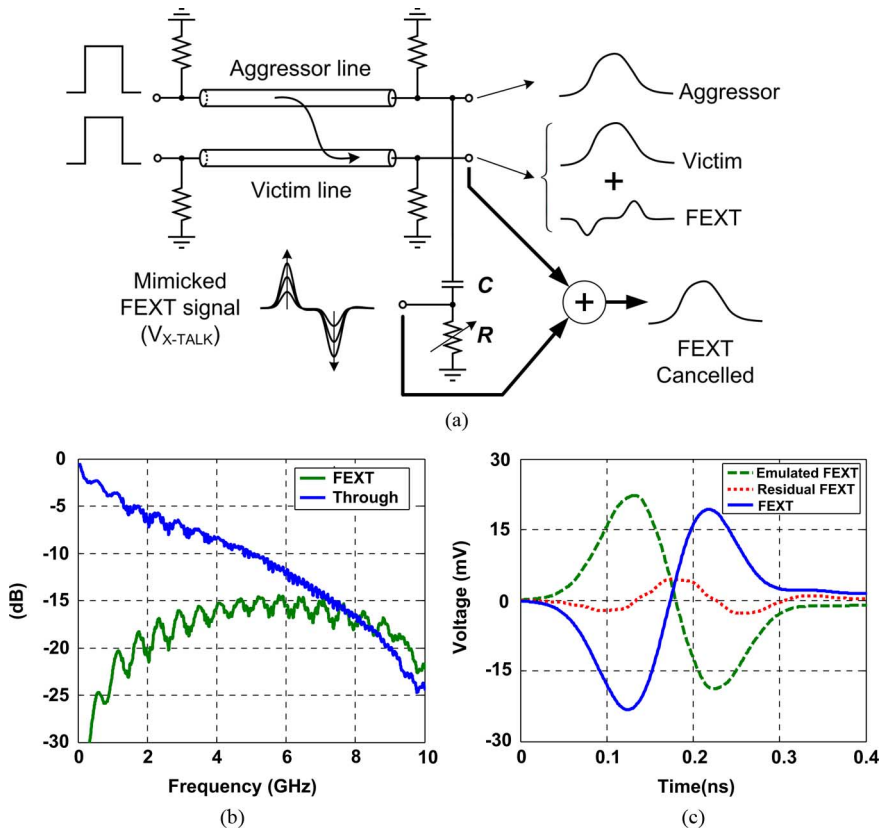


Fig. 9. (a) Crosstalk cancellation technique employing a high-pass filter as a differentiator to emulate FEXT. (b) Measured transfer characteristics of a 5-in-long, 32-mil-wide coupled trace with 40-mil separation. (c) Simulated FEXT noise due to a 15-Gb/s pulse and the emulated FEXT employing the differentiator along with the residual FEXT noise.

victim signal. For a pair of matched terminated lossless transmission lines, FEXT can be expressed by [17]

$$V_{\mathrm{FEXT}} = \frac{1}{2}\left(Z_c C_m - \frac{L_m}{Z_c}\right) l \left[\frac{dV(t-T_D)}{dt}\right] \qquad (13)$$

where $V(t)$ is the driven pulse, T_D is the delay in the medium, Z_c is the characteristic impedance, C_m and L_m are the mutual capacitance and inductance per unit length, respectively, and l is the length of the lines. For lossy microstrips, the above equation can still be used when corrected by the attenuation. The key observation from (13) is that FEXT noise appears at the front-end of the victim channel receiver as a voltage proportional to the derivative of the transmitted signal. This signal can have the same or opposite polarity as the aggressor signal if the link is capacitive or inductive, respectively.

Equation (13) shows that a differentiator with adjustable gain can be employed at the receiver to mimic the effect of FEXT. In the proposed design, the incoming aggressor signal is sent through an adjustable high-pass filter (Fig. 9) to emulate FEXT for different levels of coupling. A simple RC with variable R is employed as the high-pass filter. The variable resistor is realized by an nMOS transistor operating in triode region. If the input frequency is well below the cutoff frequency, the transfer function of the high-pass filter can be approximated by that of a differentiator with a gain equal to the time constant (RC) of the filter. The output of the differentiator is finally subtracted from the received signal, which is comprised of the desired victim signal and the FEXT, as shown in Fig. 9(a). Fig. 9(b) shows the transfer characteristics of a coupled line on FR-4 with 40-mil spacing and 32-mil width. The simulated FEXT and the output of the high-pass filter for this channel, along with the residual FEXT noise are shown in Fig. 9(c). The mimicked FEXT signal experiences a delay when it passes through the high-pass filter. As a result of this delay between the mimicked FEXT and the FEXT, the effect of the crosstalk noise is not completely eliminated. As the operating data rate is much smaller than the cutoff frequency of the filter, the amount of delay introduced is not considerable. For channels with high coupling, the gain of the filter (RC) has to be increased which results in a large delay and hence degradation of the crosstalk cancellation. The dual-path sampling technique described in Section III (Fig. 6) can be employed to resolve this problem as it can increase the filter gain while keeping the RC value constant.

In general, for dense parallel links, we may need to consider the effect of crosstalk from distant lines as well as the neighboring line. When differential signaling is employed, the crosstalk from one line to another diminishes approximately by a factor of D^{-3}, where D is the distance between the aggressor and the victim signal [13]. To investigate the functionality of the crosstalk cancellation technique in case of multiple channels, we employed three differential channels in parallel where each pair of the differential channels are 32 mil wide and spaced 32 mil while they are 48 mil apart from the adjacent channel

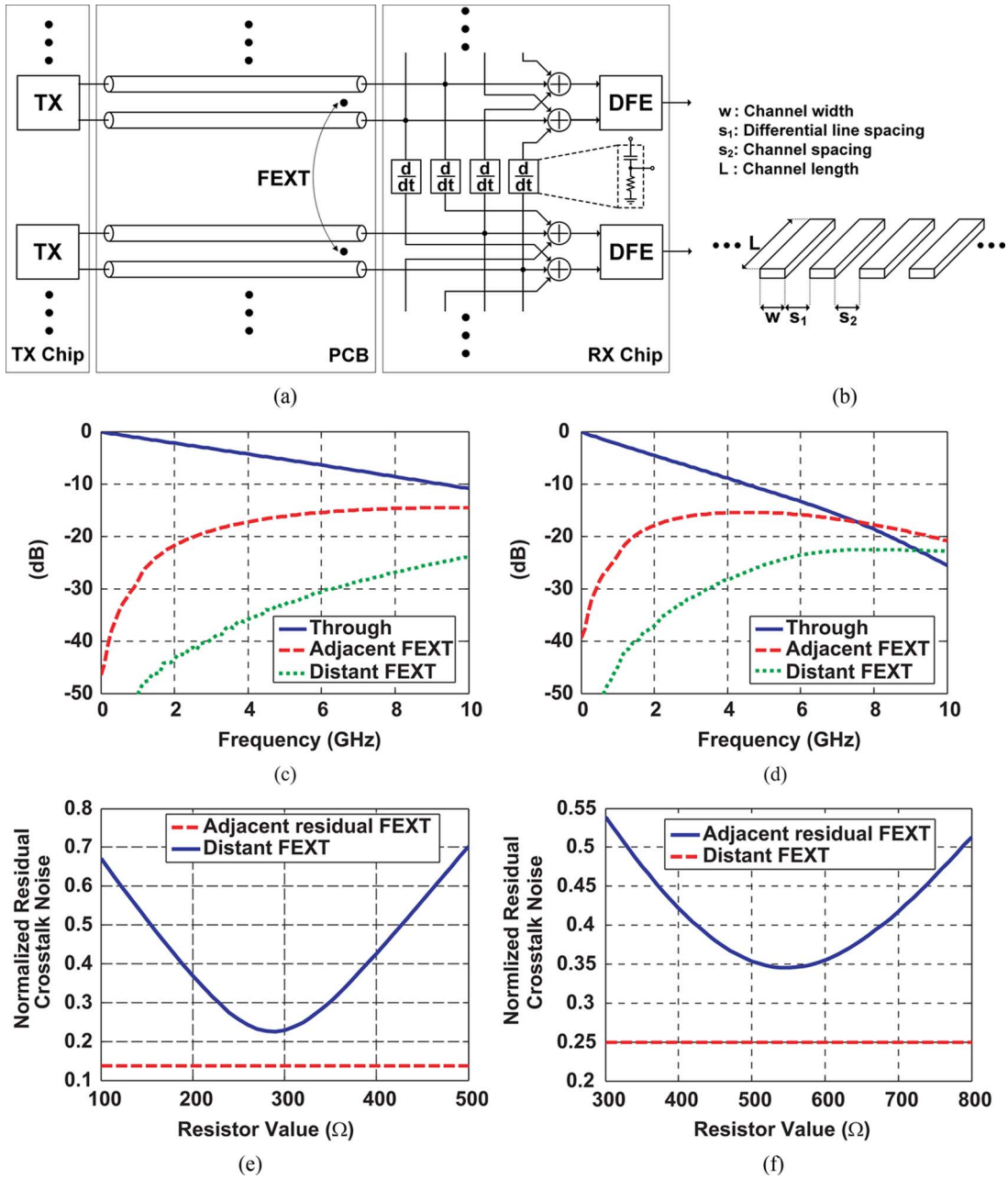


Fig. 10. (a) Crosstalk cancellation technique for multiple channels. (b) Channels cross section. (c) Simulated channel, adjacent FEXT, and distant FEXT response for $w = 32$ mil, $s = 48$ mil, and $L = 10$ in. (d) $L = 20$ in. (e) Residual crosstalk from the adjacent aggressor after cancellation normalized to the FEXT energy along with the distant FEXT for 10-in channel and (f) 20-in channel.

pair [Fig. 10(b)]. Fig. 10(c) and (d) shows the simulated transfer characteristics for the channels with 10-in and 20-in length. It can be seen that the distant FEXT is considerably lower than the adjacent FEXT. The effectiveness of the crosstalk cancellation technique was determined by normalizing the root mean square (rms) power of the residual FEXT noise to the FEXT signal rms power. With optimal selection of the differentiator gain, more than 75% reduction in crosstalk noise can be achieved. Fig. 10(e) and (f) shows the energy of the residual adjacent FEXT and the distant FEXT normalized to the FEXT energy for the 10-in and 20-in channel. The effect of the distant FEXT is less than the residual FEXT after the crosstalk cancellation is applied.

Fig. 10(a) shows how the proposed crosstalk cancellation technique can be extended to multiple differential channels in parallel. As the effect of distant crosstalk is negligible, only the effect of crosstalk from the neighboring channel is canceled by taking the derivative of the signal received at the end of the adjacent line and subtracting it form the received signal in the victim line. As a result, there will be two differentiators connected at the end of each line. The loading effect of the differentiator is small compared to the parasitic capacitance of the bonding pad. In addition, as the aggressor line is 50-Ω terminated, the resulting insertion loss due to the crosstalk sensing is negligible. Fig. 11 shows that the loading from the differentiator adds less than 0.2 dB to the overall insertion loss.

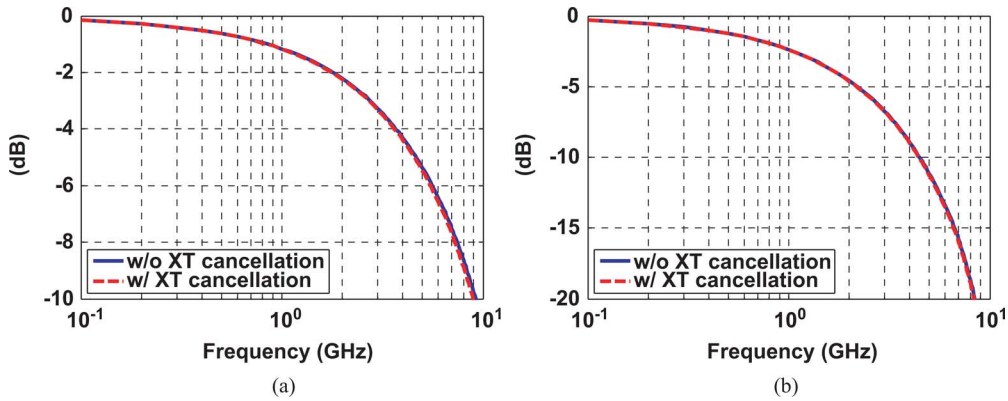


Fig. 11. Effect of loading due to the crosstalk cancellation circuitry on the overall channel insertion loss for (a) 10-in channel and (b) 20-in channel.

The proposed crosstalk cancellation method does not involve resolving the aggressor signal to compensate for its effect on the victim signal. The effect of FEXT is removed by addition of the mimicked FEXT signal to the sampled input signal during the sum/hold phase. As addition and subtraction have minimal power overhead in this architecture, crosstalk cancellation adds very small power overhead, which is mainly due to the clock buffers. In addition, this scheme is not sensitive to the phase delay between the transmitted aggressor and the victim signals, as the effect of FEXT and the mimicked FEXT are sampled at the same time. As a result, synchronization between the aggressor and victim signals is not necessary, that is, the crosstalk cancellation operates whether the aggressor transition happens in the middle of the victim bit time (center of the eye) or when the victim signal transitions.

In order to adjust the crosstalk cancellation gain, *RC*, algorithms such as BER-based adaptation can be employed [15]. To apply this technique for a lossy coupled channel, the eye closure due to crosstalk should be decoupled from the eye closure due to ISI. As a result during the adaptation process the equalization tap coefficients should be first determined by disabling the adjacent aggressor. When the tap coefficients for all channels are set by the adaptation algorithm, the adjacent aggressors are enabled and the same adaptation algorithm sets the crosstalk cancellation gain to achieve the minimum BER and hence maximum eye-opening.

V. Measurement Results

The prototype was fabricated in 45-nm SOI CMOS technology. The die micrograph is shown in Fig. 12. The receiver, consisting of clock buffers, S/H/summer, slicer/MUX and DACs, occupies 220 μm $\times$ 65 μm. Fig. 13 shows the measurement setup. The prototype was tested with different channels. Initially, the performance of the receiver was evaluated using input data with low level of ISI. The PRBS7 data was transmitted to the receiver through low-loss cables and RF probes. Under this condition, the receiver operated error-free (BER $< 10^{-12}$) up to 20 Gb/s with an input sensitivity of 100 mV, which reduces to 50 mV at 15 Gb/s. The input-referred

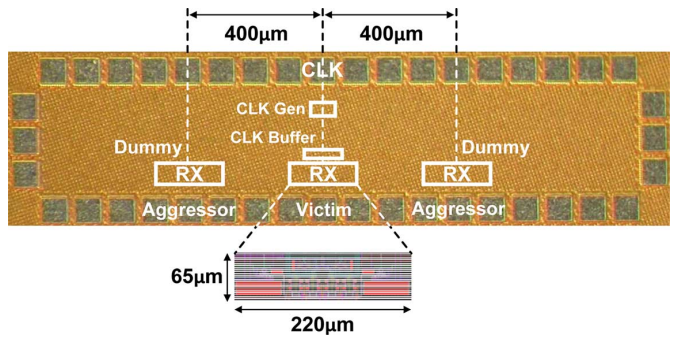


Fig. 12. Die micrograph of the receiver with major blocks highlighted.

offset was measured to be about 20 mV at 15 Gb/s. Note that offset compensation techniques are not incorporated into this design. The equalization capability of the receiver was tested by transmitting data over 5-in, 10-in, and 18-in FR-4 PCB traces. Fig. 14(a) shows the characteristics of the channels, including the connecting SMA cables and connectors. With an 800 mV_{pp} differential PRBS7 data signal at 15 Gb/s, the received eye is closed for all of these channels, shown as insets in Fig. 14. The 5-in channel exhibits a loss of 14.5 dB at 7.5 GHz. Employing the two-tap DFE, while consuming 7.5 mW from a 1.2-V supply, a 24% horizontal eye opening (BER $= 10^{-12}$) is achieved. The DFE was also tested with 10-in and 18-in channels. Due to the increased loss of the 10-in channel at 7.5 GHz, the DFE failed to equalize pseudorandom data at 15 Gb/s. The data rate was accordingly reduced to test the limits of the DFE, and 13-Gb/s data was transmitted over the 10-in channel with 17 dB of loss at 6.5 GHz. Under these conditions, the DFE achieved 35% horizontal eye opening while dissipating 6.1 mW. In order for the DFE to equalize the 18-in channel, the data rate was further reduced to 11 Gb/s. This channel had about 21 dB loss at 5.5 GHz. The DFE achieved a 26.5% eye opening while consuming 5.5 mW. In this design, the clock distribution network was not optimized for minimum power consumption. An optimized clocking system can greatly improve the power efficiency of the receiver. Simulation shows that an optimized design can reduce clocking power consumption by a factor of 2 and achieve less than 0.35 mW/Gbps power efficiency. Table I summarizes the DFE performance

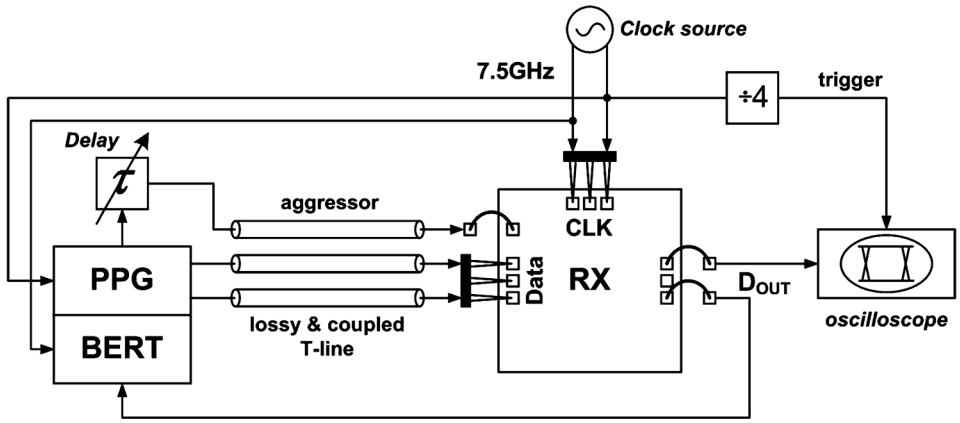


Fig. 13. Receiver DFE and crosstalk cancellation test setup.

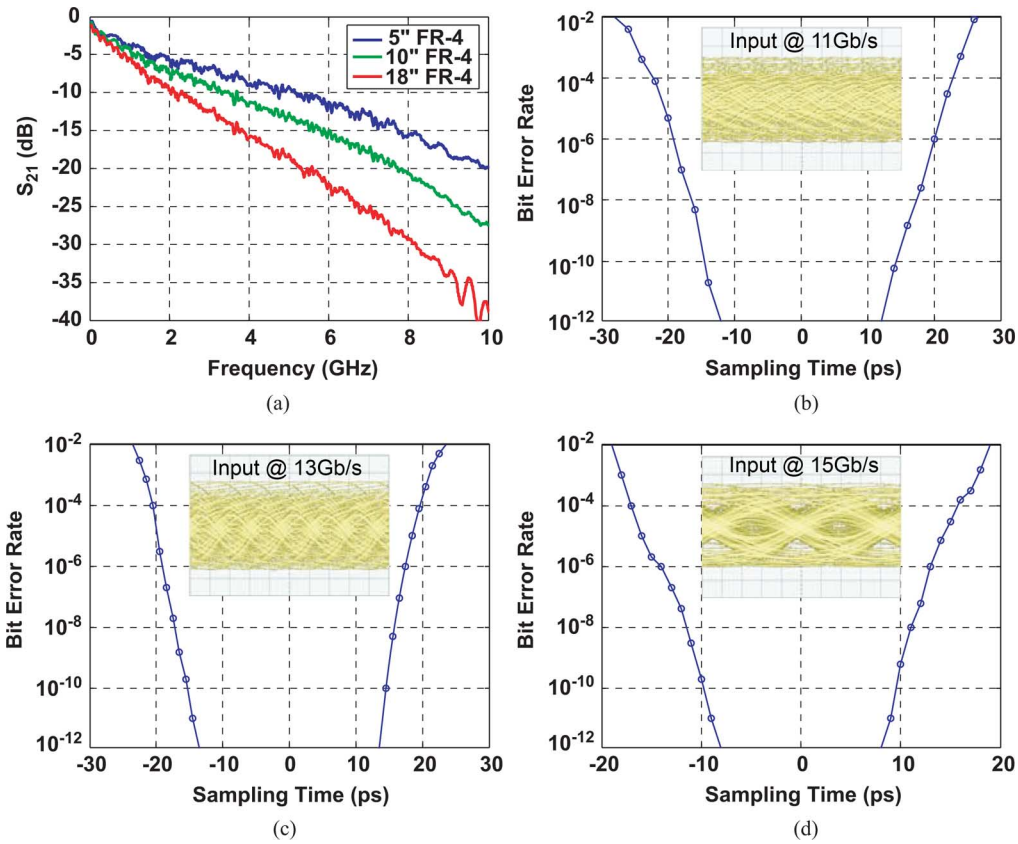


Fig. 14. (a) Channel transfer characteristics for 5-in, 10-in, and 18-in PCB traces. The PRBS7 eye diagram at the receiver input and the bathtub curve after equalization for (b) 11-Gb/s data over 18-in trace, (c) 13-Gb/s data over 10-in trace, and (d) 15-Gbs data over 5-in trace.

and compares it with prior art, showing that this design offers the best figure of merit (FOM). It also provides one of the most compact DFE designs among recently published works.

The crosstalk cancellation scheme was evaluated by transmitting random, uncorrelated victim and aggressor data over a 5-in-long, 32-mil-wide coupled trace with 40-mil separation on an FR-4 PCB. To generate uncorrelated data sequences, differential outputs of a pulse pattern generator (PPG) were delayed with respect to one another through the delay element, τ, as shown in Fig. 13. The functionality of the crosstalk cancellation technique was tested at different data rates. In the first experiment, 8-Gb/s PRBS data was transmitted over the coupled channel, while the aggressor was kept quiet. Fig. 15(a) shows that, without crosstalk noise, the DFE generates 59% of eye opening. Applying the aggressor signal degrades the eye opening to less than 40%, which is restored to above 53% when the crosstalk cancellation is activated. Next, 10-Gb/s data was employed to test the crosstalk cancellation functionality. Fig. 15(b) shows the bathtub curve of the receiver with the DFE activated to compensate for the channel loss. Applying the aggressor signal causes BER degradation to higher than 10^{-10}. Crosstalk cancellation restores the eye opening. The same experiment was repeated

TABLE I
DFE PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR ART

Reference	This work*			[2]	[3]	[4]		[5]	[6]	[7]	[8]
Process	45nm SOI			65nm	90nm	45nm SOI		90nm	45nm SOI	32nm SOI	90nm
Architecture	2-tap speculative DFE			DFE-IIR	1-tap FFE	5-tap DFE		2-tap DFE	CTLE+ 1-tap DFE	CTLE+8-tap DFE	CTLE+1-tap DFE
Supply (v)	1.2			1.0	1.4	1.0		1.0	1.2	1.1	1.0
Power (mW)	7.5	6.1	5.5	6.8	69	11	10.1	9.3	13.2	32.5	40
Data Rate (Gb/s)	15	13	11	10	16	12	9.0	7.0	20	12.5	20
Channel loss @ Nyquist (dB)	14.5	17	21	23.2	22	15	25	15	26.3	27	24
Horizontal eye opening (BER<)	24% $<10^{-12}$	35% $<10^{-12}$	26.5% $<10^{-12}$	45% $<10^{-9}$	30% $<10^{-12}$	32% $<10^{-8}$	44% $<10^{-8}$	45% $<10^{-8}$	26% $<10^{-8}$	50% $<10^{-12}$	36% $<10^{-12}$
FOM (pJ/bit)	0.5	0.47	0.5	0.68	4.3	0.92	1.12	1.33	0.66	2.6	2
Sensitivity	50mV (no offset cancellation)			32mV	N/A	93mV		31mV	N/A	N/A	N/A
Area (mm^2)	0.014			0.017	0.063	0.004**		0.019	0.012	0.055	0.09

*Excluding FEXT cancellation

**Excluding DACs for the five taps

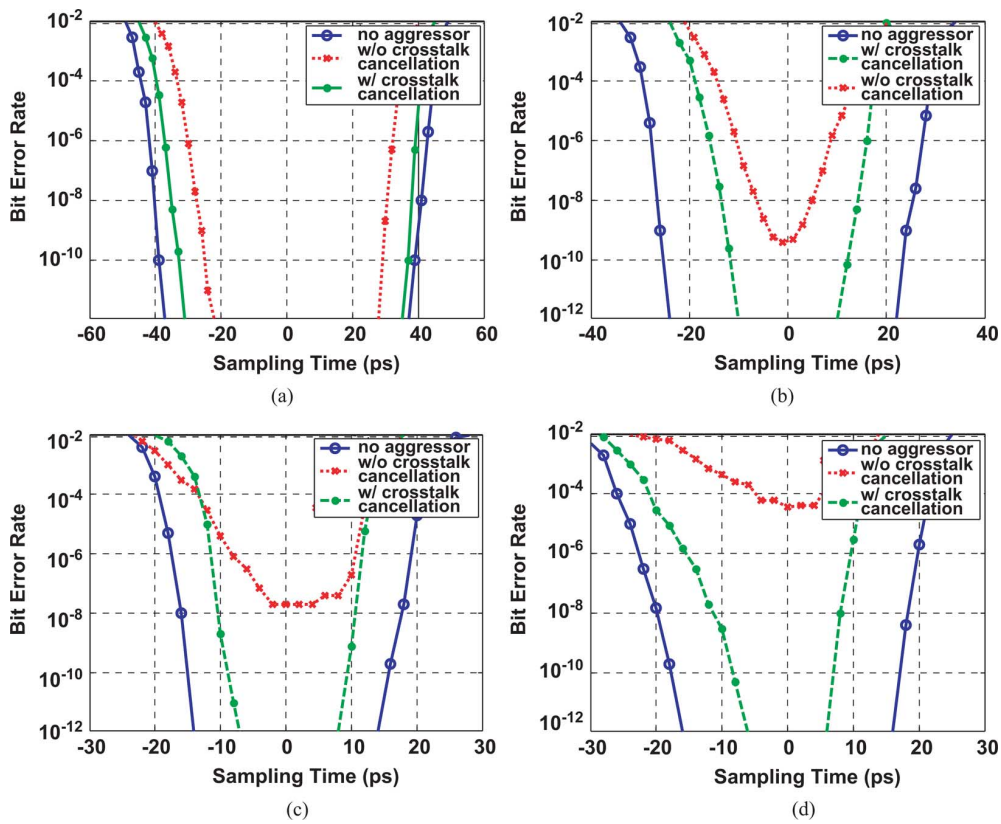


Fig. 15. Receiver bathtub curve without and with crosstalk noise, and after crosstalk cancellation for (a) 8-, (b) 10-, (c) 11-, and (d) 12.5-Gb/s victim and aggressor data.

for 11-Gb/s and 12.5-Gb/s data rates. The channel has more than 11.5-dB loss and about −15.6 dB coupling at 5.5 GHz. The DFE and crosstalk canceller provide more than 16.5% of horizontal eye opening while the input eye is completely closed due to channel loss and crosstalk noise. The values of FEXT and channel loss at 6.25 GHz are −15 and 12.5 dB, respectively. The input eye is closed when no aggressor is applied. The DFE compensates for the loss and generates a 40% open

TABLE II
CROSSTALK CANCELLATION PERFORMANCE SUMMARY

Data Rate (Gb/s)	8	10	11	12.5
Horizontal eye opening ($<10^{-12}$) no aggressor	59%	46%	31%	40%
Horizontal eye opening ($<10^{-12}$) w/o cancellation	40%	0%	0%	0%
Horizontal eye opening ($<10^{-12}$) w/ cancellation	53%	20%	16.5%	15%

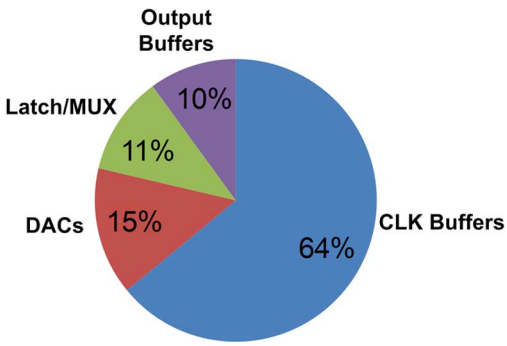


Fig. 16. Receiver power breakdown.

eye at BER $< 10^{-12}$. Applying the aggressor closes the eye and degrades the BER to higher than 10^{-5} at the center of the eye, as shown in Fig. 15(d). The crosstalk canceller achieves more than 15% horizontal eye opening. Table II summarizes the performance of the crosstalk cancellation technique.

VI. CONCLUSION

A two-tap DFE receiver with crosstalk cancellation capability is designed and fabricated in 45-nm SOI CMOS technology. It has been shown that the proposed SC DFE can be extended to implement a large number of taps. The receiver is suitable for channels with considerable amount of ISI and crosstalk noise. The simple, low-power DFE can significantly enhance the data rate over lossy channels. In this design, high-power efficiency (0.5 mW/Gb/s) is achieved by using SC summation technique, analog multiplexers, and half-rate clocking. Unlike current-mode summers, the SC summer does not require a high bias current. It can also benefit from technology scaling due to switch performance improvement and reduced power consumption of the clock distribution network. As shown in Fig. 16, the major part of the receiver power consumption is due to the clock buffers. As a result, the overall power consumption can be greatly reduced by technology scaling. A novel crosstalk cancellation is incorporated in the receiver that removes more than 75% of crosstalk noise. As addition and subtraction have minimal power overhead in the SC summer architecture, the extra hardware required for crosstalk cancellation results in only 5% (33 μW/Gbps) extra power dissipation. By multiplexing analog instead of digital signals, the number of digital latches is minimized. The half-rate clocking allows the use of CMOS clock buffers instead of CML buffers and relieves the speed requirements of the front-end circuits. Experimental results validate the feasibility of the DFE receiver for ultralow-power, high-data rate and highly parallel I/O links.

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