

A 25Gb/s 170 μ W/Gb/s Optical Receiver in 28nm CMOS for Chip-to-Chip Optical Communication

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Abstract — A low-power high-speed optical receiver in 28nm CMOS is presented. The design features a novel architecture combining a low-bandwidth TIA front-end, double-sampling technique and dynamic offset modulation. The low-bandwidth TIA increases receiver's sensitivity while adding minimal power overhead. Functionality of the receiver was validated and the design is compared with a conventional 3-stage TIA receiver via actual measurements. The proposed receiver architecture achieves error-free operation ($BER < 10^{-12}$) at 25Gb/s with energy efficiency of 170fJ/b while the conventional receiver achieves error-free operation at 17.1Gb/s with energy efficiency of 260fJ/b.

Index Terms — high-speed transceivers, hybrid integrated circuits, optical interconnection, sampled-data circuits.

I. INTRODUCTION

As bandwidth requirements for chip-to-chip interconnection scale, deficiencies of electrical channels become more severe. Parallel optical signaling has been subject of many investigations as a low-power alternative [1]. Advanced silicon photonic techniques promise low-cost and efficient integration of dense arrays of optical devices with CMOS electronics [2], [3]. Exploiting the full potential of these new technologies imposes various design challenges on optical receiver electronics.

Conventional optical receiver front-ends such as transimpedance amplifiers (TIA) require large power consumption to achieve high bandwidth and low noise, and can occupy large area due to bandwidth-enhancement techniques that require inductors. More recent techniques abandon full bandwidth approaches and use equalization techniques such as decision feedback equalization (DFE) [4] or dynamic offset modulation [5]. A DFE-based front-end can have low power consumption and good sensitivity but suffers from speed limitations due to the delay of the loop [4]. Dynamic offset modulation has power and speed benefits but has limited sensitivity performance [5].

In this work, we propose a compact low-power optical receiver, which takes full advantage of the properties of silicon-photonic devices and deep submicron CMOS technologies to achieve high speed and good sensitivity. The prototype for the proposed architecture has been implemented in a 28nm CMOS technology. A silicon

photonic chip with ultra-low capacitance photodetectors was wire-bonded to the electronic chip. The hybrid-integrated system is fully tested and measured. For comparison purposes, a conventional 3-stage TIA front-end is also implemented and its performance is measured.

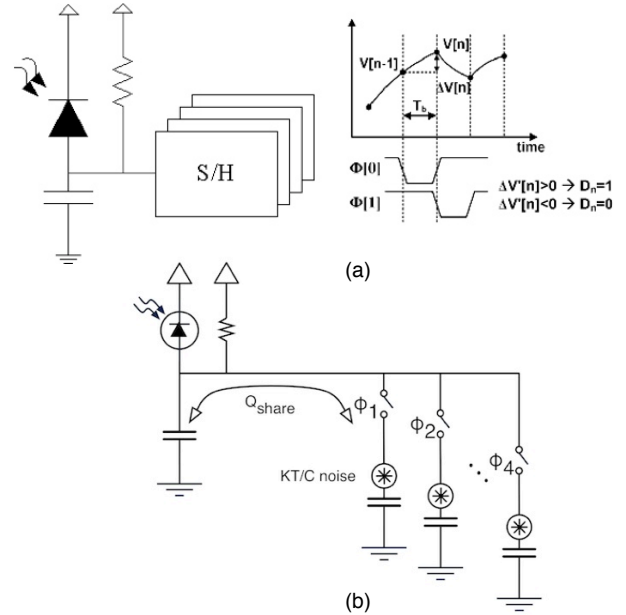


Fig. 1. (a) Double-sampling with resistive front-end used in prior art. (b) Charge sharing and KT/C noise limiting receiver's performance.

II. RECEIVER ARCHITECTURE

If a simple resistor is used to convert the current of a photodiode to a voltage, for a target SNR and a given photodiode capacitance, the input time constant (RC) severely limits the bandwidth and data rate of the receiver. In order to increase the RC bandwidth while maintaining the same gain, TIAs are commonly employed. The overall bandwidth of conventional TIAs is chosen to be $(RC)^{-1}$. Such high-bandwidth TIAs are highly analog, power hungry and do not scale well with technology.

A more recent approach uses an integrating front-end and a resistor termination with a time constant that is

much larger than the bit interval ($RC \gg T_b$) [5]. Dynamic offset modulation is then used to provide a constant voltage at its input regardless of the data sequence. The problem with this approach is that the charge integrated on the front-end capacitor gets shared with sampling capacitors (Fig. 1), causing not only sensitivity degradation, but also, limiting the lower limit for the photodiodes capacitance [5].

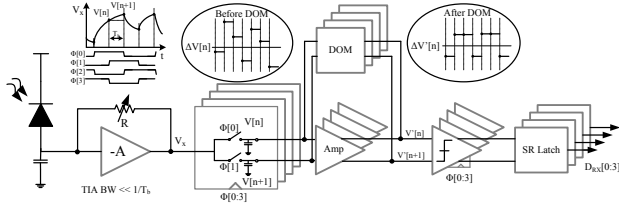


Fig. 2. Architecture of the receiver front-end with a LBW TIA.

In this work, we propose to add an ultra-low-power TIA with a bandwidth much lower than $(1/T_b)$ to the front-end. The low bandwidth (LBW) TIA's output is then sampled at the end of two consecutive bit times (V_n, V_{n+1}) and these samples are compared to resolve each bit.

Similar to [5], double-sampling technique allows demultiplexing by using multiple clock phases and samplers (Fig. 2). If the LBW TIA is designed such that the output pole is at much lower frequency compared to $1/T_b$ and the input node is at a higher frequency compared to $1/T_b$, the dynamic offset modulation provides a constant voltage at sense-amp's input regardless of the data sequence. Fig. 2 shows the top-level architecture of the receiver. The input current from the photodiode is converted to a voltage through LBW TIA with transimpedance of $3K\Omega$. TIA's output is sampled by a bank of four sample/holds (S/H). The S/H capacitor (C_s) is chosen to be 12fF to maximize speed while minimizing noise and current sensitivity. The low-bandwidth TIA provides isolation between PD's capacitor and sampling capacitors, which reduces charge-sharing effect and enables use of ultra-low capacitance photodetectors in scaled silicon photonic technologies. Besides, for a given PD capacitance, S/H capacitors can be chosen to be bigger (even comparable to PD's capacitance) to relieve KT/C noise. This had been an important bottleneck in double-sampling optical receivers in the past [5], [6]. Sampling capacitors are followed by an amplifier with a gain of 4.5dB, which also provides isolation between sampling nodes and sense-amp to minimize kickback. The dynamic offset modulation employed at the output of the amplifier introduces an offset so that the sense-amp differential input is always constant regardless of the previous bit. The high-speed sense-amp has digital offset cancellation using a bank of 5 capacitors. The sense-amp is followed by an

SR-latch to retrieve the NRZ data. The low-bandwidth TIA's DC offset cancellation, dynamic offset modulation and amplifier all have digital calibration controllers using a seven bit current DAC (Fig. 3).

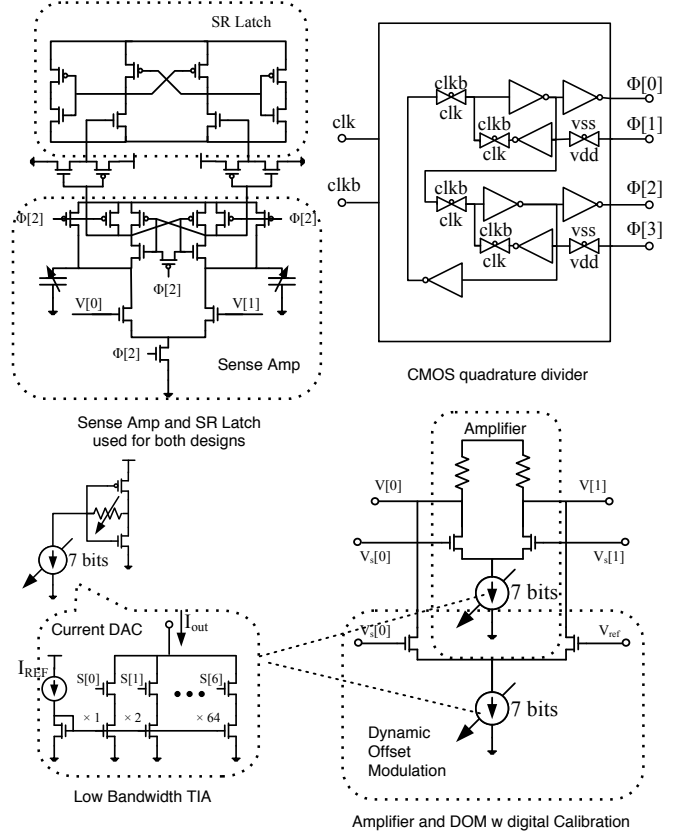


Fig. 3. Transistor-level diagram of core building blocks of proposed Architecture.

In [5] it has been shown that for a single-pole system with a dynamic offset modulation coefficient of $\beta = 1 - e^{-T_b/RC}$ the ΔV at sense-amp's input will be constant, regardless of the data sequence. In the case of LBW TIA, the system has two poles. Unlike conventional TIAs, the dominant pole is chosen to be at the output node, being $\omega_2 = 1/\tau_2 = 1/(4R_f C_{S/H})$, to minimize KT/C noise of sampling capacitors. Choosing $\beta = 1 - e^{-T_b/\tau_2}$, sense-amp input voltage will be

$$\Delta V' \approx \frac{R_f I_{pd} (1 - e^{-T_b/\tau_2})}{2(1 + 1/A)}$$

Where R_f is the TIA's feedback resistor, I_{pd} is the photodetector current, T_b is the bit time interval and A is the gain of amplifier used in the LBW TIA. The dominant pole associated with output node of the LBW TIA is at 1GHz while the input node has a pole at 5GHz.

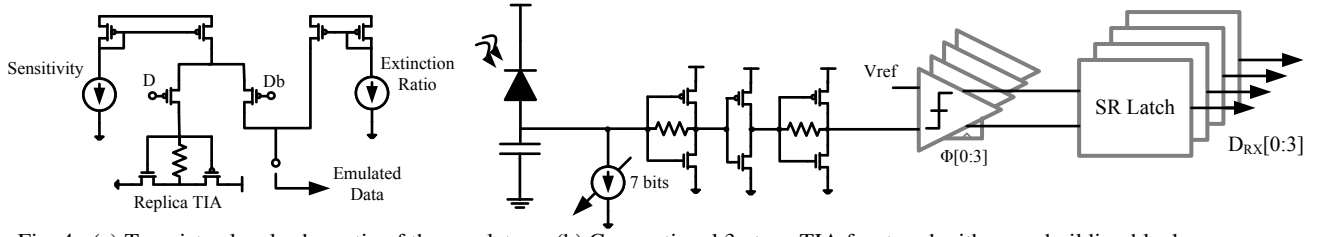


Fig. 4. (a) Transistor-level schematic of the emulator (b) Conventional 3-stage TIA front-end with same building blocks.

III. MEASUREMENT RESULTS

Two prototypes were fabricated in a 28nm CMOS technology to compare performance of the new architecture with a conventional TIA-based receiver. The 3-stage TIA architecture is similar to the one described in [2]. This design is optimized to have maximum bandwidth for the given technology (28nm CMOS). Each prototype is comprised of two receivers, one with a photodiode emulator and one for optical testing with photodetectors (Fig. 4). Both chips are designed for stand-alone testing as well as testing with integrated silicon-photonics. Fig. 5 shows the measurement setup.

First, receivers were tested using the emulator and PRBS 7,9 and 15 sequences. An on-chip bank of capacitors mimics the total parasitic capacitance at the input node (due to the photodetector, pad and bond-wire) to be 30fF in the standalone test. Fig. 6 shows how the BER changes with the input current at 12Gb/s, 16Gb/s, 20Gb/s, and 25Gb/s. The proposed architecture achieves about 20 μ A of sensitivity at 12Gb/s that drops to 55 μ A at 25Gb/s.

In comparison to the proposed design, the conventional design has a sensitivity of 23 μ A at 12Gb/s, which degrades to 75 μ A at 17.1Gb/s. While sensitivity degradation in double-sampling receiver is mainly due to reduced bit interval and integration time, in full-bandwidth approach it is due to a closed eye and therefore ISI at the sense-amps. The receivers' power consumption and energy efficiency at different data rates are shown in Fig. 7.

In both proposed and conventional designs, the power of digital elements increases linearly with speed. The conventional TIA design offers energy efficiency of

260 μ W/Gb/s at 17Gb/s compared with the proposed architecture that has efficiency of 180 μ W/Gb/s at 17Gb/s. Efficiency of the proposed design reaches its peak of 170 μ W/Gb/s at 25Gb/s.

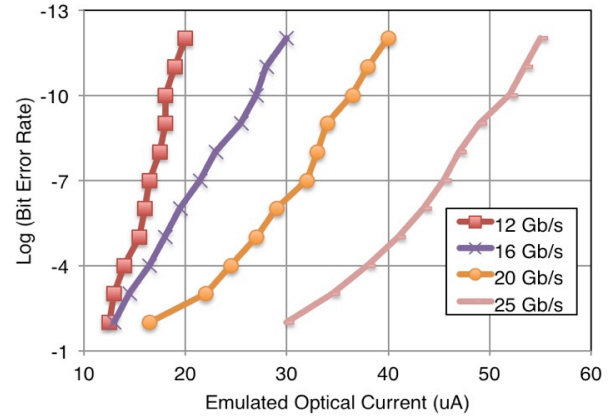


Fig. 6. Proposed receiver's sensitivity characteristics at different rates using a PRBS 7,9 and 15.

For optical testing, receivers were bonded to a silicon-photonics die with low-capacitance (8fF) photodetectors. This die has an array of waveguide-coupled photodiodes that use a grating coupler to couple light from an off-chip source. Responsivity of photodiodes is 0.8A/W at 1310nm and the total capacitance due to the photodiode, bond-wire and pad is estimated to be 30fF. The optical beam from a DFB laser diode is modulated by a high-speed Mach-Zehnder modulator and coupled to the photodiode through a single-mode fiber. Fig. 9 shows how sensitivity of the receivers changes with data rate. Note that coupling loss is not included in this plot and the actual sensitivity of the receiver is superior to these results. While the

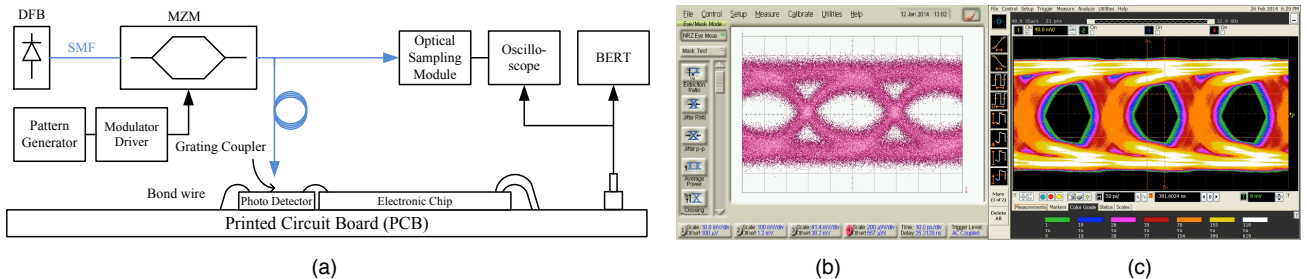


Fig. 5. (a) Optical test setup (b) Optical input eye diagram to the photo-diode at 25Gb/s and (c) SR Latch NRZ output.

conventional architecture achieves -4.8dBm of sensitivity at 17.1Gb/s (its maximum speed), the proposed architecture achieves -10.2dBm of sensitivity at 17Gb/s and -6.8dBm at 25Gb/s.

Fig. 8 shows die micrographs of the two receivers and waveguide coupled photodiode, as well as a picture of the wire-bonded test setup. The top metal layers are designed to be compatible with copper-pillar flip-chip bonding as well as bond-wire.

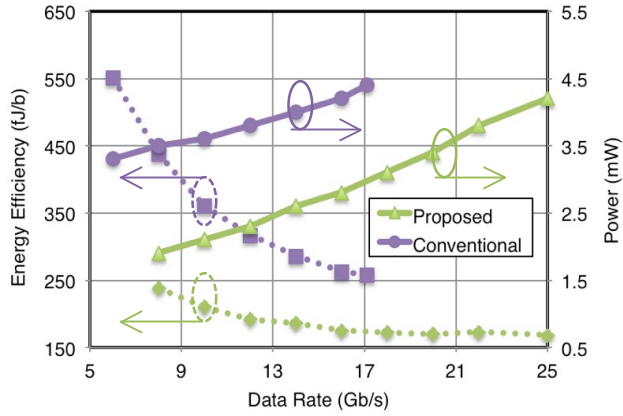


Fig. 7. Power consumption and energy efficiency of proposed and conventional architectures at different data-rates.

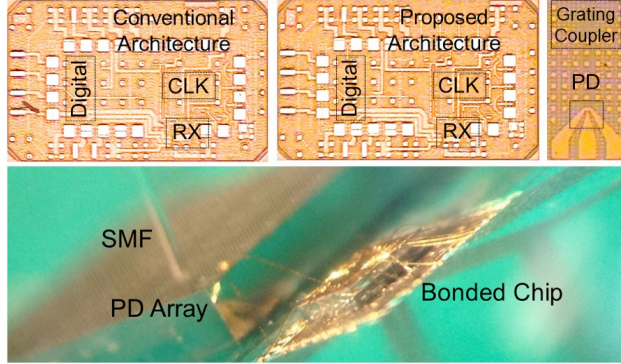


Fig. 8. Micrograph of the two CMOS receivers, waveguide coupled PD, and test setup with fiber coupled to the PD.

IV. CONCLUSION

The double-sampling optical receiver with low-bandwidth TIA and dynamic offset modulation consumes $170\mu\text{W}/\text{Gb/s}$ while operating at 25Gb/s and has an optical sensitivity of -10.2dBm at 17Gb/s, which drops to -6.8 at 25Gb/s. This architecture is well suited for hybrid integration of highly scaled integrated silicon-photonics and electronics. Experimental results validated the feasibility of the receiver as well as its superiority over conventional TIA architecture. Table 1 summarizes the

performance of the optical receiver and compares it to the state-of-the-art.

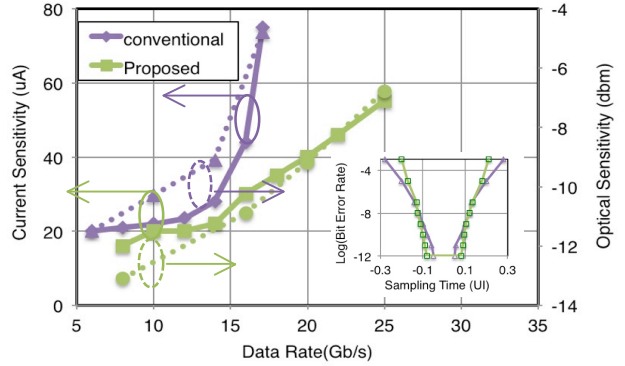


Fig. 9. Sensitivity at different rates and BER bathtub curves at 25Gbps and 17.1Gbps for proposed and conventional designs.

Table 1. Performance summary and comparison.

	New Arch.	Conv. Arch.	[2]	[5]	[6]	[7]
Technology	28nm	28nm	40nm	65nm	90nm	65nm
Data Rate (Gb/s)	25	17.1	10	24	16	28
Efficiency (mW/Gb/s)	0.17	0.26	0.395	0.4	1.4	3.25
Area (mm ²)	0.0018	0.0018	-	0.0028	0.025	0.32
RX C _{in} (fF)	<30	<30	60	<200	440	-
Sensitivity	Current (μA) @ 25Gb/s	75 @ 17Gb/s	-	160 @ 24Gb/s	284 @ 16Gb/s	86 @ 25Gb/s
	Optical (dBm) @ 25Gb/s	-4.8* @ 17Gb/s	-15** @ 10Gb/s	-4.7* @ 24Gb/s	-5.4* @ 16Gb/s	-9.7 @ 25Gb/s

* Actual optical measurements, coupling losses are not considered.

**Estimated through current sensitivity, knowing responsivity of the PD.

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